TECHNICAL BULLETIN

No. TB11-6600-252-10-1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 15 January 1979

SUPPLEMENTARY OPERATING INSTRUCTIONS

TEST SET, INTEGRATED CIRCUIT CARD

TESTERS AN/USM-371 AND AN/USM-371A

(TEST PROGRAMS FOR AUTODIN

PRINTED CIRCUIT CARDS

NO. A52602 THROUGH **A65089)**

REPORTING OF ERRORS

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1. Purpose. This technical bulletin provides supplementary instructions in the form **of** test programs and associated data for troubleshooting AUTODIN printed circuit cards No. A52062 through A65089, using Test Set, Integrated Circuit Card Tester AN/USM-371 and AN/USM-371A.

In this bulletin, the following test sets are referenced by the indicated manufacturer's model number:

Nomenclature	Model Number
AN/USM-371	Model ICT-102
AN/USM-371A	Mode1 ICT-103

2. Test Procedures. Refer to the general instructions to become familiar with the basic data required for troubleshooting the faulty printed circuit card. Locate the schematic diagram and test data that pertain to **the** faulty card. Operate the test set to isolate the fault as described in the operating procedures.

Dynatronics Products

PC CARD TEST PROGRAMS
for the
MODEL ICT-102 and ICT-103
PRINTED CIRCUIT CARD TESTER

INTEGRATED CIRCUIT CARD TEST SET
AN/USM-371 and AN/USM-371A
used for
AUTODIN PC CARDS A52602 through A65089

PROGRAM MANUAL

GENERAL DYNAMICS
Electro Dynamic Division

LIST OF EFFECTIVE PAGES

TOTAL NUMBER OF PAGES IS 143 AS FOLLOWS.

Page No.	Issue	Page No.	Issue	Page No.	Issue	Page No.	Issue
Title	Original						
A	Original						
i through iii/iv.....	Original						
1 through 137	Original						

* The asterisk indicates pages revised, added or deleted by the current change

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

TABLE OF CONTENTS (CONT'D)

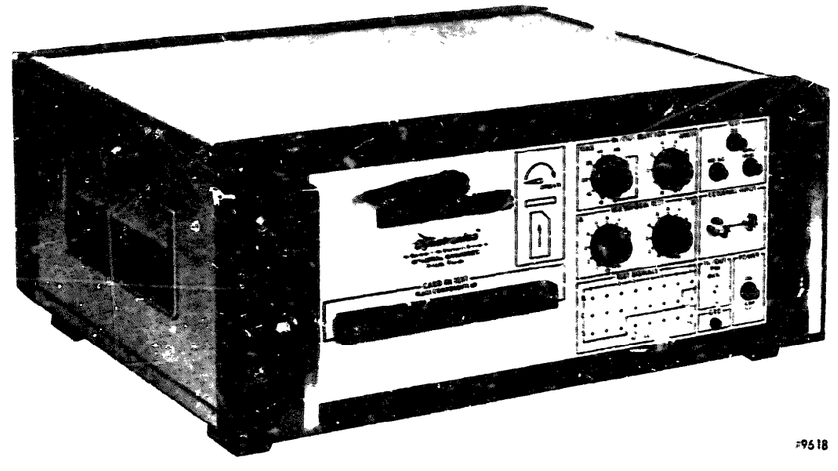
LIST OF ILLUSTRATIONS

LIST OF TABLES

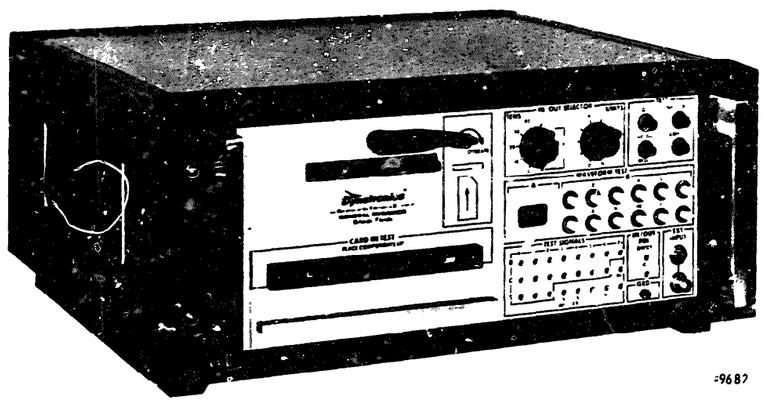
GENERAL DESCRIPTION

Dynatronics Printed Circuit Card Tester models ICT-102 and ICT-103 provide the capability for dynamically testing virtually and logic family on a visual basis. Punched Hollerith cards contain individual programs which eliminate elaborate test hook -ups normally found during testing operation. No external test equipment is necessary because complete dynamic tests are performed by the Card Tester each time an individual program cared is inserted into the card reader. All condtions (signal generation, power distribution , grounding, loading, test rates, etc.) are controlled by the program card and all circuits are fully tested by following a simple set of instructions and observing the GO/NO-GO and FAULT indicator lamps on the front panel. These instructions are provided in the following paragraphs.

Differences in the two models (ICT-102 and ICT-103) are illustrated in figure 1. Basically the card testers function alike with the main differences being in operator switch setting procedures. The model ICT-102 Card Tester uses rotary switches for selecting circuit under test output signal GO/NO-GO test parameters whereas the model ICT-103 Card Tester features pushbuttons in place of the rotary switches. Individual card test documentation provided in this manual can be used for either model Card Tester.



MODEL ICT-102 CARD TESTER



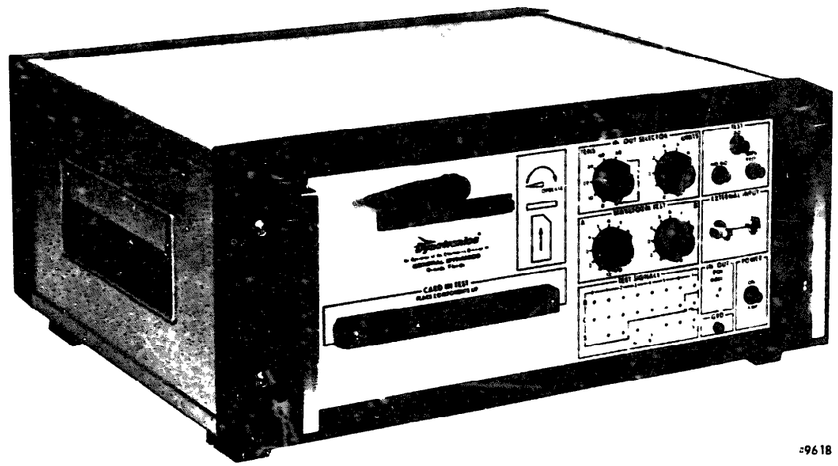
MODEL ICT-103 CARD TESTER

Figure 1. Printed Circuit Card Testers (100 Series)

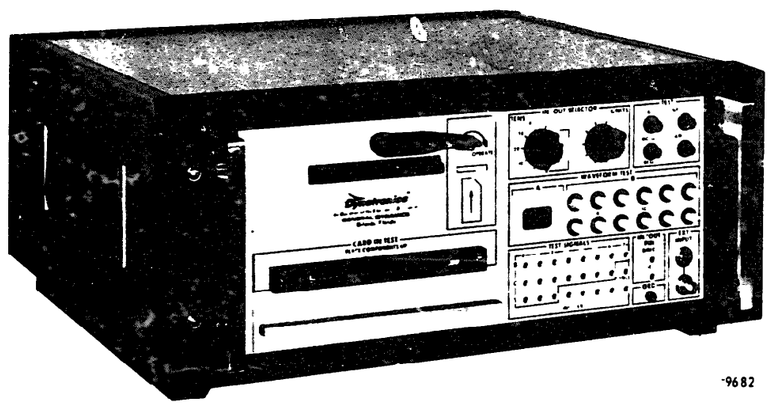
GENERAL DESCRIPTION

Dynatronics Printed Circuit Card tester models ICT-102 and ICT- 103 provide the capability for dynamically testing virtually any logic fam ily on a visual basis. Punched Hollerith cards contain individual programs which elim inate elaborate test, hook-ups normally found during testing operations. No external test equipment is necessary because complete dynamic tests are performed
Tester each time an individual program card is inserted into the card reader. All conditions (signal generation, power distribution, grounding, loading, test rates, etc.) are controlled by the program card and all circuits are fully tested by following a simple set of instructions and observing the GO/NO-GO and FAULT indicator l amps on the front panel. These instructions are provided in the following paragraphs.

Differences in the two models (ICT-102 and ICT-103) are illustratea in figure 1. Basically the card testers function alike with the main differences being in operator switch setting procedures. The model XT-102 Card Tester uses rotary switches for selecting circuit under test output signal GO/NO-GO test parameters whereas the model ICT-103 Card Tester features pushbuttons in place of the rotary switches. Individual card test documentation provided in this manual can be used for either model Card Tester.



MODEL ICT-102 CARD TESTER



MODEL ICT-103 CARD TESTER

Figure 1. Printed Circuit Card Testers (100 Series)

Each schematic or logic diagram associated with individual programmed **cards are marked such that pertinent** information related to signal routing, **power distribution, and** other test requirements are readily available to the test technician. Markings and symbols normally found on schematic or **logic diagrams are** listed below:

a. Parenthesis - Used to enclose test information such **as pin numbers and test signals generated by** the card tester and routed to the card-under-test **via the card reader, i. e . ,** (4) indicates that this pin connects to the card tester CARD IN TEST connector, pin 4; (+CO) indicates that test signal +CO is connected to the card-under-test via the card reader.

b. Symbol (H) - Placed adjacent to schematic wiring which remain at a high logic level throughout the test. A high logic level is defined as the upper level of the signal voltage levels.

c. Symbol (L) - Placed adjacent to schematic wiring which remain at a low logic level throughout the test. A low logic level is defined as the lower level of the signal voltage levels.

Note

All points not labeled (H) or (L) are dynamic i.e., are switching during the test.

d. -/- This symbol indicates input or output lines which are not tested by the card tester test program. **On cards which are tested by two** programs, the symbol indicates that the input or output line is not tested by either program.

e. (GRD) Symbol - Indicates that DC **power** ground from the card tester is applied to the card-under-test at this point,

f. **(+Vcc) Symbol** - Independent +5 ±0.5 volt power supply internal to the card tester used for supplying **+Vcc** to the car&under-test via the card test program. This power supply, +5 EXT, is adjusted from the rear panel of the card tester.

g. ±V, +V, **-V** Symbols - These symbols indicate which of the three program-mable power supplies are connected to the card-under-test. The output voltage values for the programmable power supplies are located on the waveform sheet in the TEST PARAMETERS table.

h. (NC) Symbol - Indicates that there is no connection made between the referenced point on the card-under-test and the card tester.

These markings are located on the schematic drawings where applicable and are defined in the TEST LEGEND contained on each schematic. Definitions for the above markings apply to both the ICT-102 and ICT-103 Card Testers.

CARD TESTER WAVEFORM MARKINGS

Several symbols are used on the waveform charts to indicate special procedures required while testing a particular printed circuit card. These symbols and/or special instructions are located in the notes at the bottom of each waveform chart. Before proceeding with any test it is required that the notes be read 2-3 special instructions be carried out. For example, the notes may indicate that the Card Tester +5 volt external power supply be adjusted to +4.5 volts prior to testing the printed circuit card in question. In this case the printed circuit card could be damaged if the power supply had been adjusted to +5.5 volts for the preceeding test. Typical notes and symbols are described below:

a. Asterisk * Symbol - This symbol when placed adjacent to a pin number (either input or output pin) on the waveform chart indicates that the signal on that pin is inverted with respect to the waveform shown. Typically these symbols are located in the INPUT PINS and OUTPUT PINS columns of the waveform chart.

b. # Symbol - Indicates that no further edges are present in the output signal under test and the output is tested according to the steps for the model of Card Tester in use.

c. Encircled Output Pins - Encircled output pins are **the** more significant outputs that when tested check the majority of the circuits on the card-under-test. These output pins should be tested first to determine the general status of the card being tested. For example, when testing a multiple stage shift register with individual stages brought out on pins, the last stage of the shift register would be encircled and tested before the individual stages were tested. In this manner it is determined that the card is functionally operational after checking a single output pin.

MODEL ICT-102 OPERATING PROCEDURES

Following **is** the step-by-step procedure for performing dynamic test analysis on printed circuit cards programmed for the model ICT 102 Card Tester. These instructions pertain to all printed circuit cards; specific instructions peculiar to individual printed circuit cards undergoing tests are listed as notes on the appropriate waveform sheet. Waveform sheets for individual printed circuit cards are contained in this volume. Before proceeding with any test, the operator must read the notes contained on the waveform sheet and follow any specific instructions first. In addition the necessary card adapters, card extender cables, and programmable load boards should be inserted in the Card Tester to accommodate the card to be tested. The steps listed below provide the necessary information for successful diagnostic testing of all printed circuit cards programmed for testing with the ICT-102.

a. Refer to the appropriate card under test schematic or logic diagram and corresponding waveform sheet. On the waveform sheet, locate the notes and follow the instructions pertinent to the operator. Typically. the notes are located along the bottom edge of the waveform sheet.

b. Insert the PC card adapter and/or extender cable (if required) into the CARD IN TEST connector on the front panel of the Card Tester.

C. Insert the printed circuit card to be tested into the card adapter with the component side facing up.

d. Locate the corresponding card under test program card and insert it into the card reader slot asi depicted on the front panel of the Card Tester. Push the program card into the card reader slot until there is a noticeable resistance felt against the test card. Move the card reader handle clockwise until it is in the full closed position.

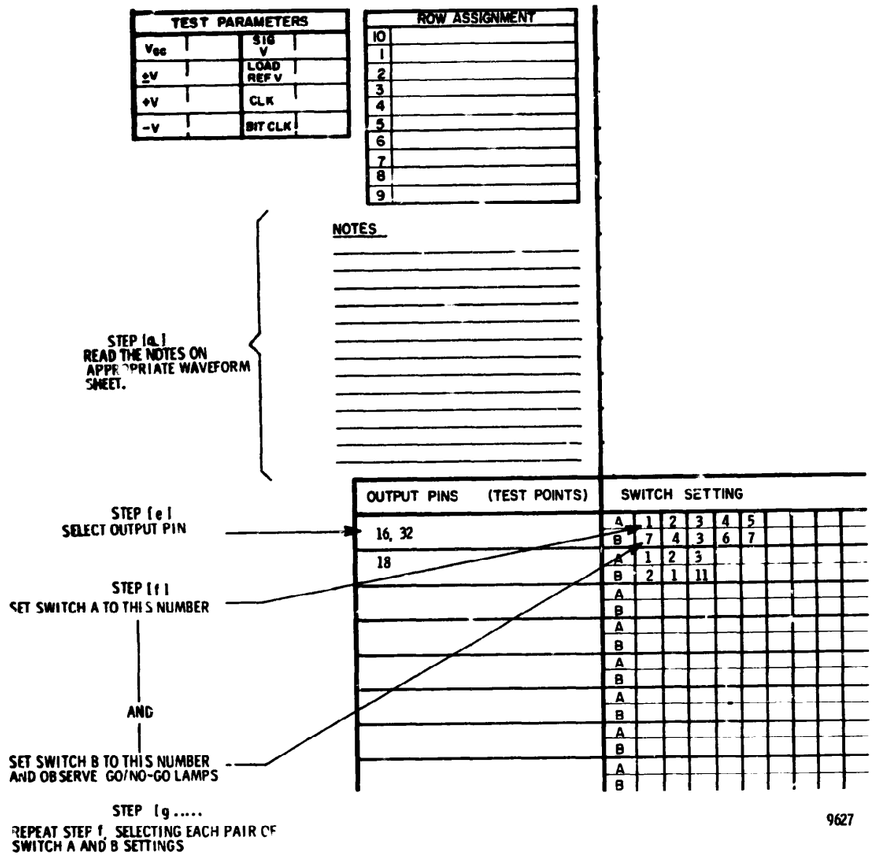


Figure 2. Model ICT-102 Waveform Sheet Example

Note

When initially energized, the Card Tester INPUT FAULT indicator is illuminated. Resetting the Card Tester should clear the INPUT FAULT indicator. If the INPUT FAULT indicator is not extinguished after resetting the Card Tester, a true input fault is present in the card-under-test and should be corrected before continuing.

e. Select the output pin to be tested on the front panel IN/OUT SELECTOR switches (S2 and S3). Figure 2 shows a typical example of an output pin (pin 16) and its location on the waveform chart.

f. Set WAVEFORM TEST switch A to the first number shown under the SWITCH SETTING heading which corresponds to the selected output pin on the waveform chart. As shown in figure 2, the number 1 would be selected by switch A.

g. Place WAVEFORM TEST switch B to the first number adjacent to SWITCH SETTING B which corresponds to the selected output pin.

h. Observe the three TEST indicators on the front panel and determine the outcome of the circuit being tested. The two possible indications are explained below:

1. GO indicator lights green - circuit being tested checks good for this measurement and the operator should continue with the next step.

2. NO-GO indicator lights red - circuit being tested does not **meet the** output requirements for the programmed test. Recheck the switch settings to ensure that there has been no operator **error** and then make the necessary notations on the card in test paper work for follow-up maintenance.

i. Place WAVEFORM TEST switches A and B to the next pair of SWITCH SETTINGS, shown on the waveform chart, and observe the TEST indicators as in the previous step, Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO,

ate

A # symbol in the last “B” switch setting position indicates that a NO-GO indication should be observed for all “B” switch settings (1 through 12). A GO indication in any of these positions indicates a malfunction (more edges than required).

j. Change both IN/OUT SELECTOR switches to the next output pin number located on the waveform char, either adjacent to the output just tested or, if there is no adjacent number, to the next output pin number directly below the output pin just tested.

k. Place. WAVEFORM TEST switches A and B to each pair of corresponding SWITCH SETTING numbers. Continue this procedure until all settings for a given output Pin have been carried out and all test indications have been GO. Repeat steps (j .) and (k.) Until all output pins **and corresponding** SWITCH SETTINGS have been tested.

1. Rotate the card reader handle **counter-clockwise to the full open position,** remove the Program card from the card reader slot and insert the test card into the appropriate plastic card holder.

m. Determine whether or not the card under test requires additional testing using another program test card. **If** additional testing is required, repeat steps (a .) through (m.) for the additional test (s) . If **no** further testing is required, remove the tested printed circuit card from the card adapter.

MODEL ICT-103 OPERATING PROCEDURES

Following is the step-by-step procedure for performing dynamic test analysis on printed circuit cards programmed for the model ICT-103 Card Tester. These instructions pertain to all printed circuit cards: specific instructions peculiar to individual printed circuit cards undergoing tests are listed as notes on the appropriate waveform sheet. Waveform sheets for individual printed circuit cards are contained in this volume. Before proceeding with any test, the operator must read the notes contained on the waveform sheet and follow any specific instructions first. In addition the necessary card adapters, card extender cables, and programmable load boards should be inserted in the Card Tester to accommodate the card to be tested. The steps listed below provide the necessary information for successful diagnostic testing of all printed circuit cards programmed for testing with the ICT-103.

a. Refer to the appropriate card under test schematic or logic diagram and corresponding waveform sheet. On the waveform sheet, locate the notes and follow the instructions pertinent to the operator. Test notes are normally located along the bottom edge of the waveform sheet.

b. Insert the PC card adapter and/or extender cable (if required) into the CARD IN TEST connector on the front panel of the Card Tester.

c. Insert the printed circuit card to be tested into the card adapter with the component side facing up.

d. Locate the corresponding card-under-test program card and insert it into the card reader slot as depicted on the front panel of the Card Tester. Push the program card into the card reader slot until there is a noticeable resistance felt against the test card. Move the card reader handle clockwise until it is in the full closed position.

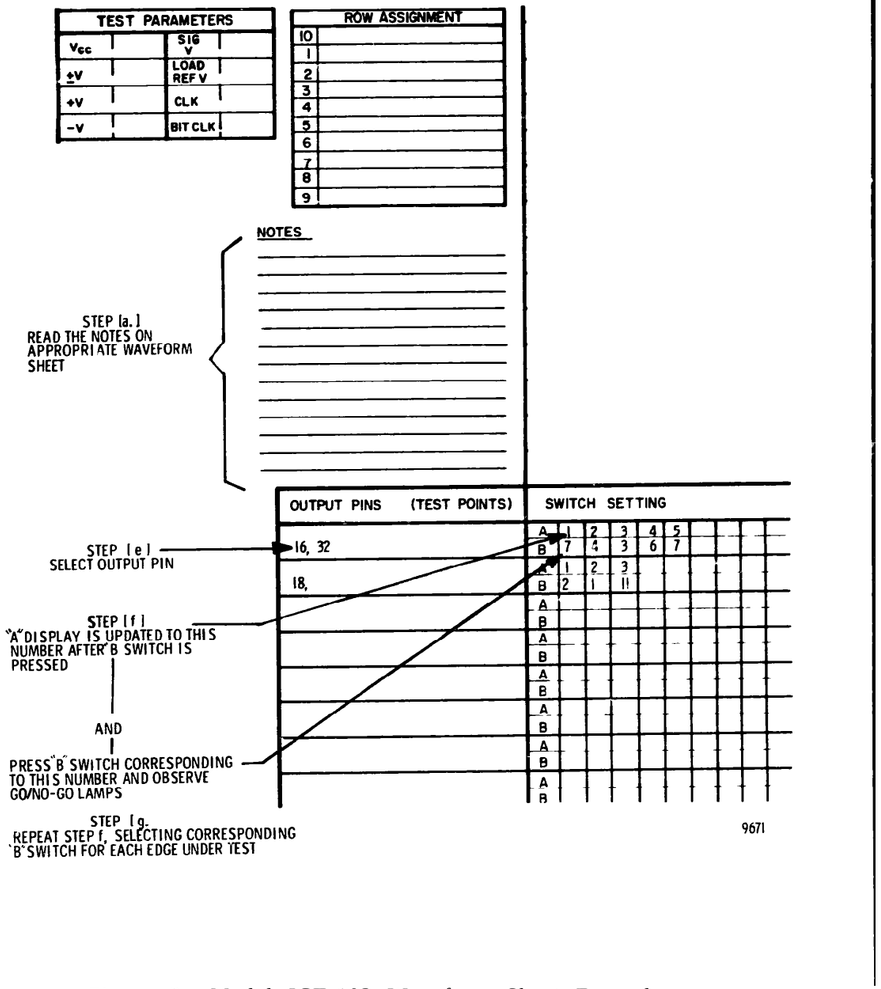


Figure 3. Model ICT-103 Waveform Sheet Example

Note

If the INPUT FAULT indicator is lit, press the RESET switch. If the INPUT FAULT indicator is not extinguished after resetting the Card Tester, a true input fault is present in the card-under-test and should be corrected before continuing.

e. Select the output pin to be tested on the front panel IN/OUT SELECTOR switches (S2 and S3). Figure 3 shows a typical example of an output pin (pin 16) and its location on the waveform chart.

f. WAVEFORM TEST “A” display should read 0 (left digit blank). If the “A” display does not read zero, press the reset switch/indicator.

g. Press the WAVEFORM TEST “B” switch corresponding to the first number adjacent to SWITCH SETTING B (figure 3) which corresponds to the selected output pin (switch number 7 in this example). WAVEFORM TEST display “A” changes to (01).

h. Observe the three TEST indicators on the front panel and determine the outcome of the circuit being tested. The two possible indications are explained below:

1. GO indicator lights green - circuit being tested checks good for this measurement and the operator should continue with the next step.

2. NO-GO indicator lights red - circuit being tested does not meet the output requirements for the programmed test. Recheck the switch settings to ensure that there has been no operator error and then make the necessary notations on the card in test paper work for follow-up maintenance.

i. Press WAVEFORM TEST switch B which corresponds to the next B SWITCH SETTING, shown on the waveform chart, and observe the TEST indicators as in the previous step. Each time a B switch is press the A display is incremented one count. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO.

j. Change both IN/OUT SELECTOR switches to the next output pin number located on the waveform chart either adjacent to the output just tested or, if there is no adjacent number, to the next output pin number directly below the output pin just **tested.**

Note

A # symbol in the last “B” switch setting position indicates that GO test result should occur after “B” switch “#" is depressed. If a NO-GO indication is observed after pressing “B” switch “#", the circuit being tested has malfunctioned.

k. Press WAVEFORM TEST switch B for each pair of corresponding SWITCH SETTING numbers. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO. Repeat steps (j.) and (k.) until all output pins and corresponding SWITCH SETTINGS have been tested.

1. Rotate the card reader handle counter-clockwise to the **full open position, remove the program card** from the card reader **slot and insert the test card into the appropriate** plastic **card holder.**

m. Determine whether or not the card under test requires **additional testing using** another program test card. If additional testing **is required, repeat steps (a** .) through (m.) for the additional test (s). If no further testing is required, remove the tested printed circuit card from the card adapter.

Note

In some instances, the GO/NO-GO test documentation may skip "A" display counts to enable the operator to ignore "don't care" transitions in the waveform under test. For example, consider the following:

A	1	2	3	4	5	6	7
B	6	9	NT	NT	3	6	10

Where NT = NO TEST

The operator would press the "B" switches in the following sequence: B-6 A=1), B-9 (A=2), B-3 three times (steps A to count 5) B-6 (A=6), B-10 **A = 7.**

SPECIAL CONSIDERATIONS

JUMPERS

Jumpers are required occasionally while performing tests on printed circuit cards for bypassing passive components or otherwise routing DC voltages within the card-under-test. **These jumpers should be carefully placed on** the **card-under-**test prior to inserting the program **card (energizing the** Card **Tester) into the Card** Tester and should be checked **to ensure proper placement. Information concerning** placement of jumpers is located in the notes at the bottom of the appropriate waveform **test diagram snd on the schematics or logic diagrams.**

+5 EXT POWER SUPPLY ADJUSTMENT

Four power supply output voltages are available in the Card Tester which can be applied to the card-under-test. Three of these power supplies are controlled by the program test card and the fourth, the +5 Volt EXT power supply, is adjusted by the operator according to the individual test programs. When adjusting the +5V EXT power supply to accommodate different printed circuit card families, care should be taken to adjust the output voltage within ± 100 millivolts of the recommended voltage. Exceeding the 100 millivolt tolerance can cause erroneous readings on the Card Tester GO/NO-GO indicators, as described below.

Erroneous readings caused by maladjusted power supply voltages is normally due to the RC timing circuits present on many cards. A large voltage variation in either direction will cause a significant change in the **duration of** the timed interval, and may result in an erroneous "B" switch count. This phenomena is illustrated in Figure 4, along with the timing variations imposed by the tolerances on the resistor and capacitor values. The curves were generated for the circuit shown in figure 4.The switching threshold of gate Y was found

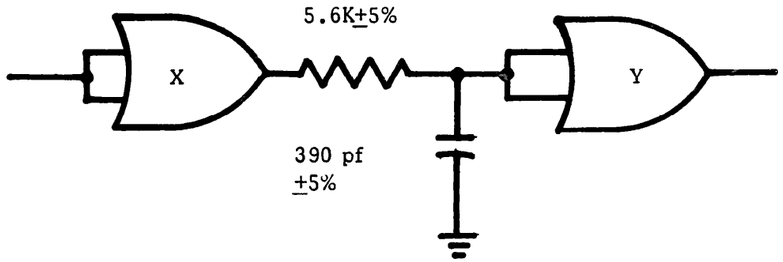


Figure 4. Typical RC Network

to remain nearly constant at approximately 2.O volts as the supply voltage was varied from 4.50 to 5.OO volts.

It is seen in Figure 5 that with Vcc = 4.75 and nominal RC values, Gate Y will switch 1.68 used after the output of Gate X goes to the high state. With VCC = 5.00 and the resistor and capacitor values at the low end of the tolerance range, Gate Y will delay 1.43 used before switching. With Vcc = 4.50 and the timing components at the high end of the tolerance range, Gate Y will delay 2.05 used before switching. Thus, it is seen that for curves A and B, a “B” switch count of 2 would be obtained: while an erroneous "B" switch count of 3 would be obtained for the conditions represented by curve C.

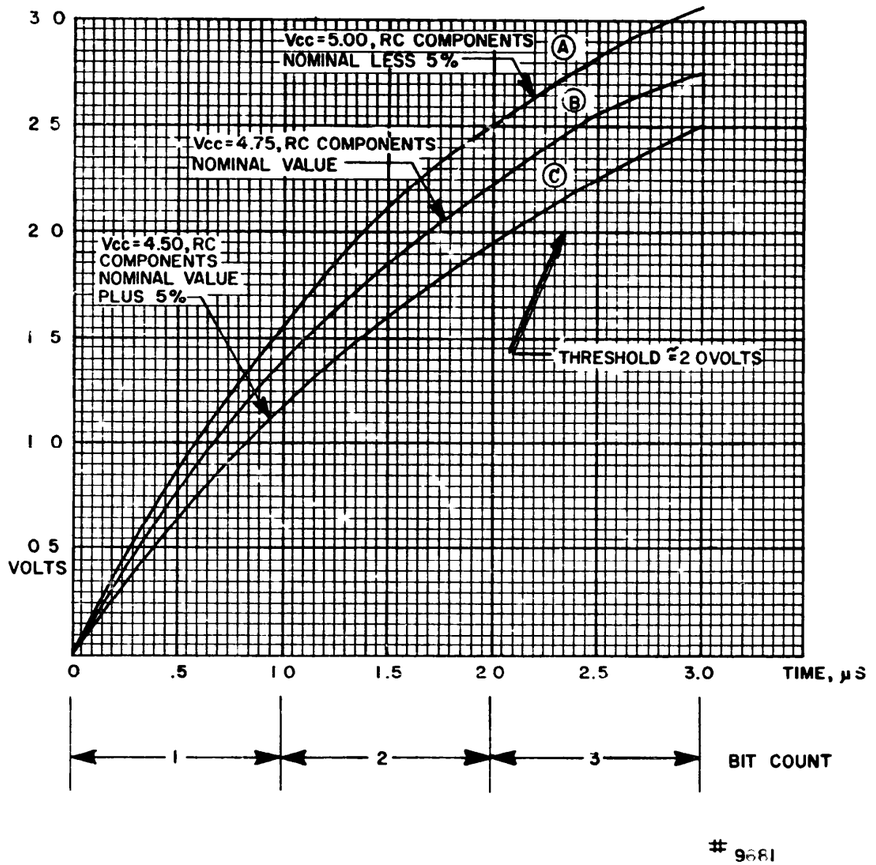


Figure 5. Voltage Tolerance Versus Time Delay Chart

For cases where the time delay circuit is isolated from other circuitry it would usually be possible to program around the problem discussed above. However on many cards, several timing circuits operate in series such that while one programming technique may provide a wide margin of safety for one circuit in the series, it may reduce the margin of safety for another timing circuit in the series. Therefore it is desirable to reduce the magnitude of error of the controllable variables such as supply voltage which determine the duration of the timed intervals.

Note

The above conditions also affect the pulse duration of slivers (spikes) noted in some program waveforms. These spikes are not tested by the Card Tester (too narrow for detection) and are not critical with respect to the logic circuit operation. In most cases the spikes are less than 10 nanoseconds in duration and in some cases are hardly discernable from one Card Tester to the next.

PRINTED CIRCUIT CARD ADAPTERS

Several printed circuit card adapters are available to interconnect between the Card Tester and various printed circuit card families contained in this manual. Following is a cross-reference table of the individual card adapters and associated printed circuit card family. Pin number cross-reference and card adapter identification for individual PC card adapters are provided in the following tables and illustrations .

Table 1. Printed Circuit Cord Adapters

DYNATRONICS PART NO.	MILITARY NOMENCLATURE	ADAPTS CARD TESTER TO:
12-890051	MX-9089/USM-371	23 Pin Anelex
12-890052	MX-9090/USM-371	44/88 Pin Anelex
12-890053	MX-9091/USM-371	22 Pin SN-394 (RED)
12-890054	MX-9092/USM-371	26 Pin SN-394 (BLACK)
12-890056	MX-9093/USM-371	22 Pin MD-674
12-890059	MX-9094/USM-371	43/86 Pin FGC
12-890055	MX-9095/USM-371	60 Pin TCU
12-890050	MX-9096/USM-371	46 Pin GDE
12-890058	MX-9097/USM-371	25 Pin FGC

Table 2. Printed Circuit Card Adapter MX-9089/USM-371
Pin Cross Reference

ADAPTER MX-9089/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9089/USM-371	CARD TESTER PIN NUMBER
1	46	12	35
2	45	13	34
3	44	14	33
4	43	15	32
5	42	16	31
6	41	17	30
7	40	18	29
8	39	19	28
9	38	20	27
10	37	21	26
11	36	22	25
		23	24

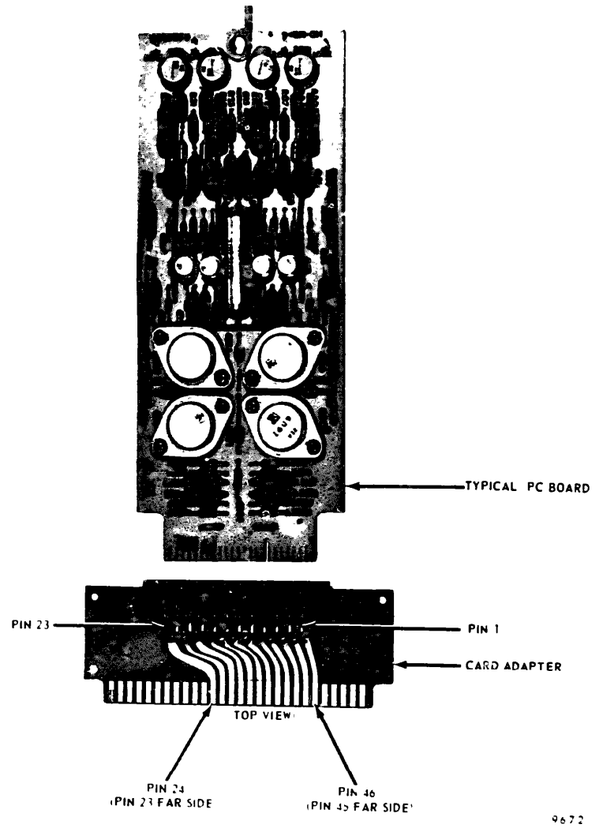


Figure 6. Printed Circuit Card Adapter MX-9089/USM-371
(23 Pm Anelex)

Table 3. Printed Circuit Card Adapter MX-9090/USM-371
Pin Cross Reference

ADAPTER MX-9090/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9090/USM-371	CARD TESTER PIN NUMBER
1	55	23	36
2	53	24	34
3	51	25	32
4	49	26	30
5	47	27	28
6	45	28	26
7	43	29	24
8	41	30	22
9	39	31	20
10	37	32	18
11	35	33	16
12	33	34	14
13	31	35	12
14	29	36	10
15	52	37	8
16	50	38	6
17	48	39	4
18	46	40	2
19	44	41	54
20	42	42	
21	40	43	50
22	38	44	

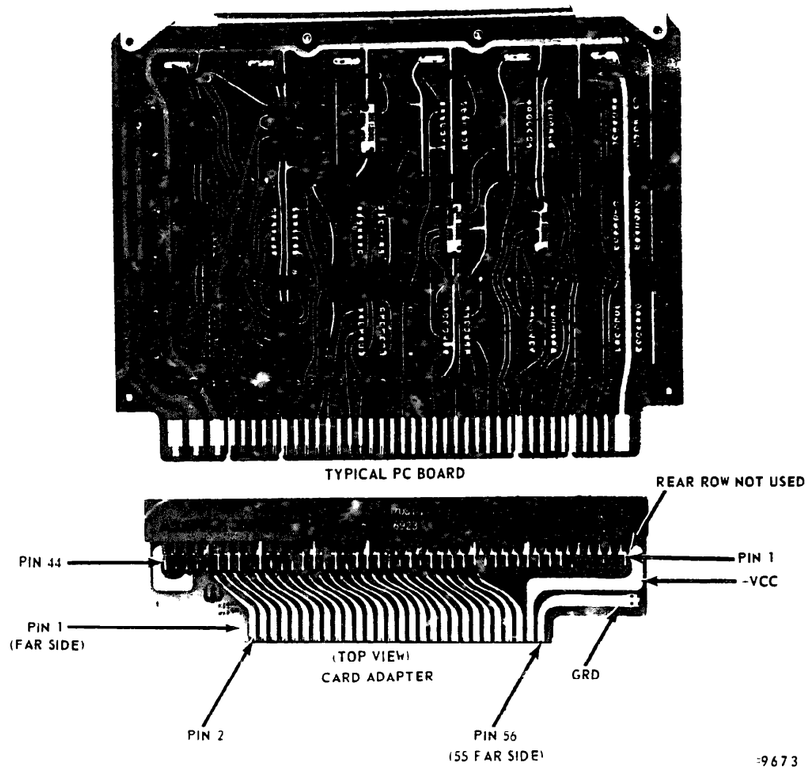


Figure 7. Printed Circuit Card Adapter MX-9090/USM-371
(44/88 Pm Anelex)

Table 4. Printed Circuit Card Adapter MX-9091/USM-371
Pi n Cross Reference

ADAPTER MX-9091/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9091/USM-371	CARD TESTER PIN NUMBER
1	22	12	11
2	21	13	10
3	20	14	9
4	19	15	8
5	18	16	7
6	17	17	6
7	16	18	5
8	15	19	4
9	14	20	3
10	13	21	2
11	12	22	1

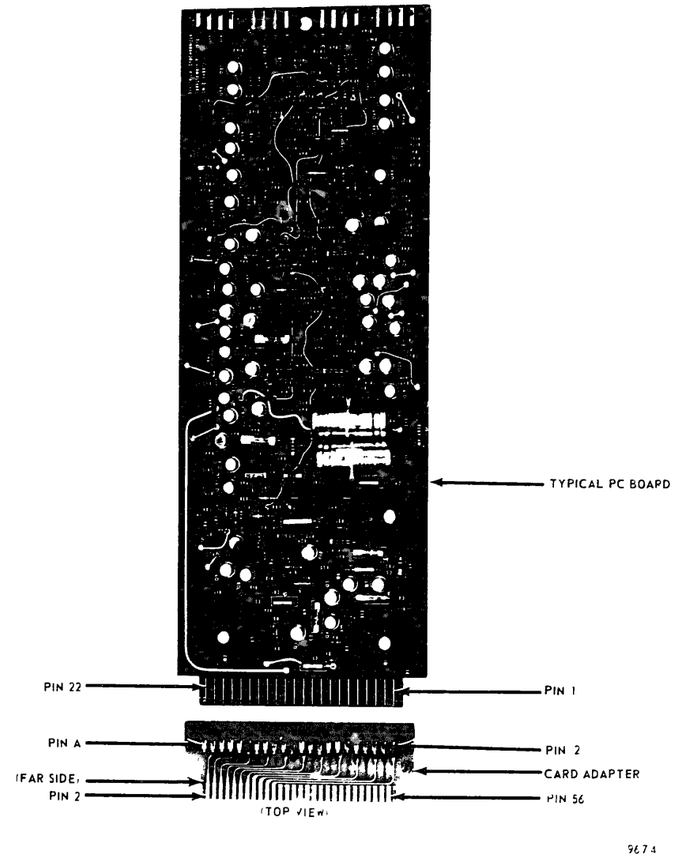


Figure 8. Printed Circuit Card Adapter MX-9091/USM-371
22 Pm SN-394 (Red)

Table 5. Printed Circuit Card Adapter MX-9092/USM-371
Pm Cross Reference

ADAPTER MX-9092/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9092/USM-371	CARD TESTER PIN NUMBER
1	52	29	26
2	51	30	25
3	50	31	24
4	49	32	23
5	48	33	22
6	47	34	21
7	46	35	20
8	45	36	19
9	44	37	18
10	43	38	17
11	42	39	16
12	41	40	15
13	40	41	14
14	39	42	13
15	38	43	12
16	37	44	11
17	36	45	10
18	35	46	9
19	34	47	8
20	33	48	7
21	32	49	6
22	31	50	5
23	30	51	4
24	29	52	3
25	28	53	2
26	27	54	1

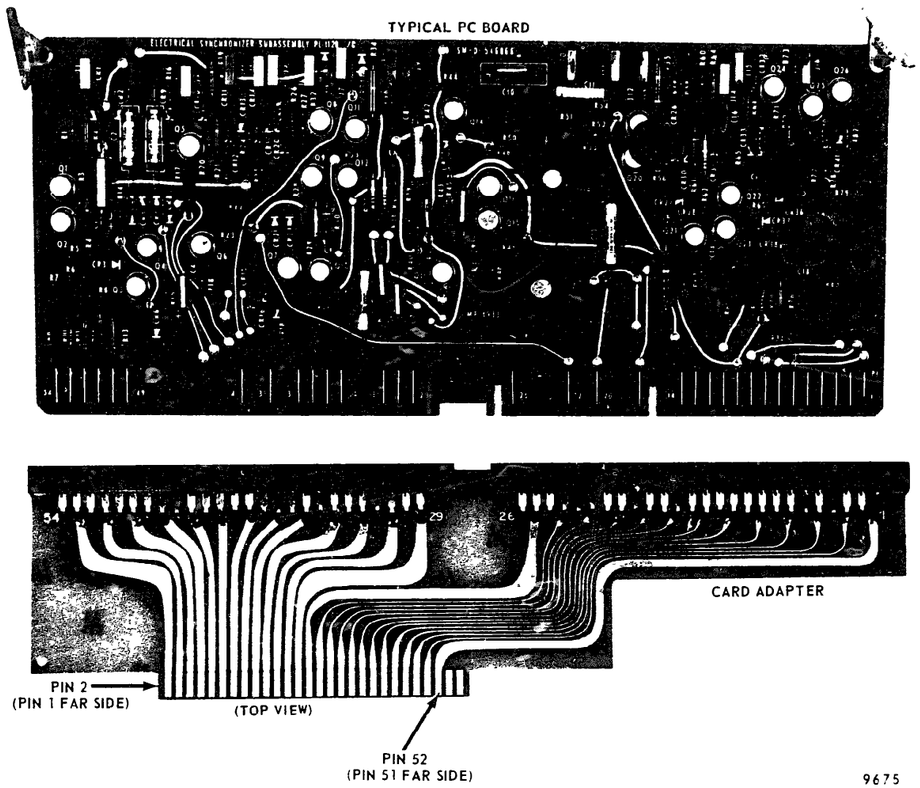


Figure 9. Printed Circuit Card Adapter MX-9092/USM-371
26 Pin SN-394 (Black)

Table 6. Printed Circuit Card Adapter MX-9093/USM-371
Pin Cross Reference

ADAPTER MX-9093/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9093/USM-371	CARD TESTER PIN NUMBER
A	1	N	12
B	2	P	13
C	3	R	14
D	4	S	15
E	5	T	16
F	6	U	17
H	7	V	18
J	8	W	19
K	9	X	20
L	10	Y	21
M	11	Z	22

#G, I, O, Q - omitted

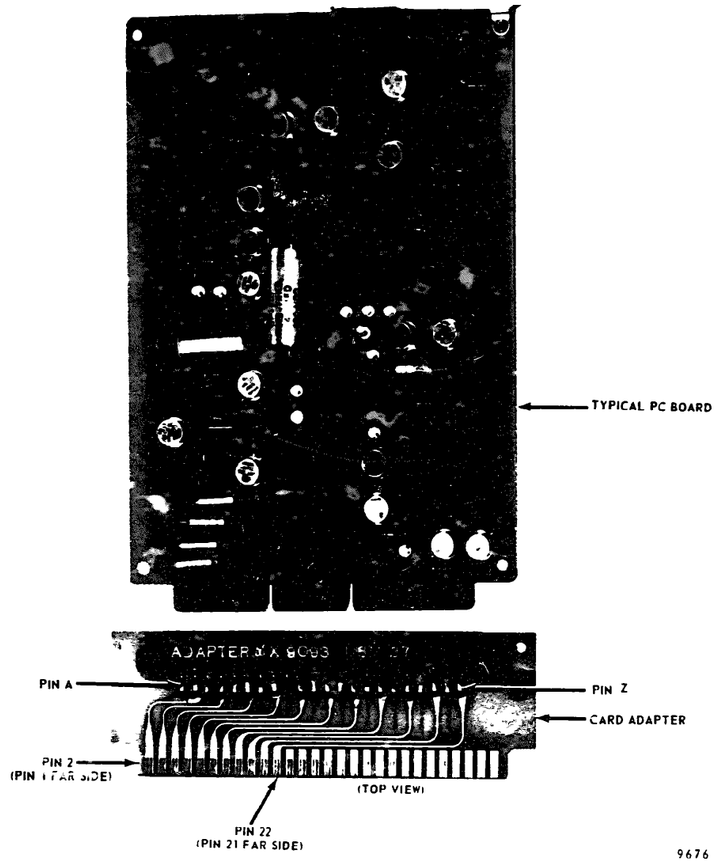


Figure 10. Printed Circuit Card Adapter MX-9093/USM-371
22 Pin MD-674

Table 7. Printed Circuit Card Adapter MX-9094/USM-371
Pin Cross Reference

ADAPTER MX-9094/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9094/USM-371	CARD TESTER PIN NUMBER
1	1	45	23
3	2	47	24
5	3	49	25
7	4	51	26
9	5	53	27
11	6	55	28
13	7	57	29
15	8	59	30
17	9	61	31
19	10	63	32
21	11	65	33
23	12	67	34
25	13	69	35
27	14	71	36
29	15	73	37
31	16	75	38
33	17	77	39
35	18	79	40
37	19	81	41
39	20	83	42
41	21	85	43
43	22		

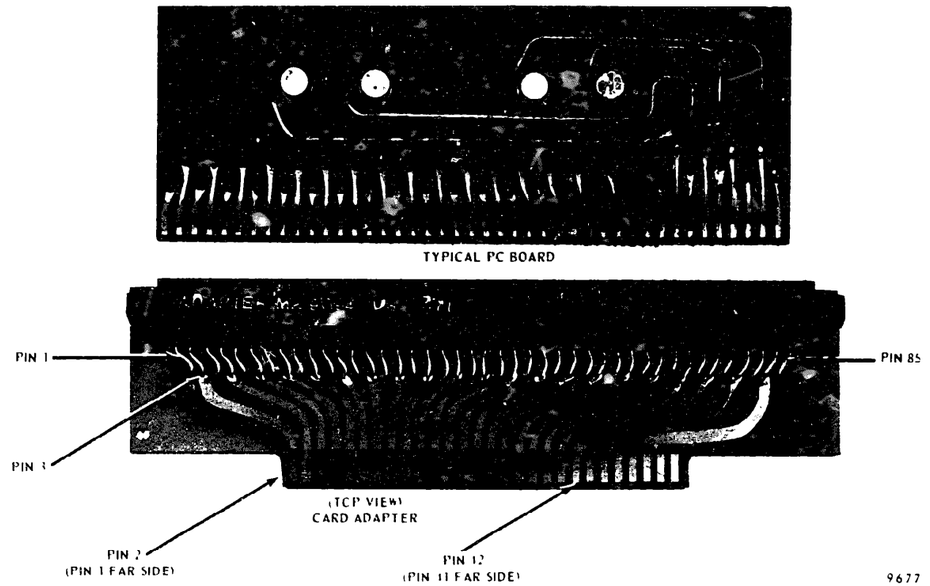


Figure 11. Printed Circuit Card Adapter MX-9094/USM-371

13/86 Pm FGC

Table 8. Printed Circuit Card Adapter MX-9095/USM-371
Pin Cross Reference

ADAPTER MX-9095/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9095/USM-371	CARD TESTER PIN NUMBER
1	56	31	54 (+5V)
2	51	32	No connection
3	No connection	33	55
4	49	34	53
5	47	35	52
6	45	36	50
7	43	37	48
8	41	38	46
9	39	39	44
10	37	40	42
11	35	41	40
12	33	42	38
13	31	43	36
14	29	44	34
15	27	45	32
16	25	46	30
17	23	47	28
18	21	48	26
19	19	49	24
20	17	50	22
21	15	51	20
22	13	52	18
23	11	53	16
24	9	54	14
25	7	55	12
26	5	56	10
27	3	57	8
28	No connection	58	6
29	No connection	59	4
30	1	60	2

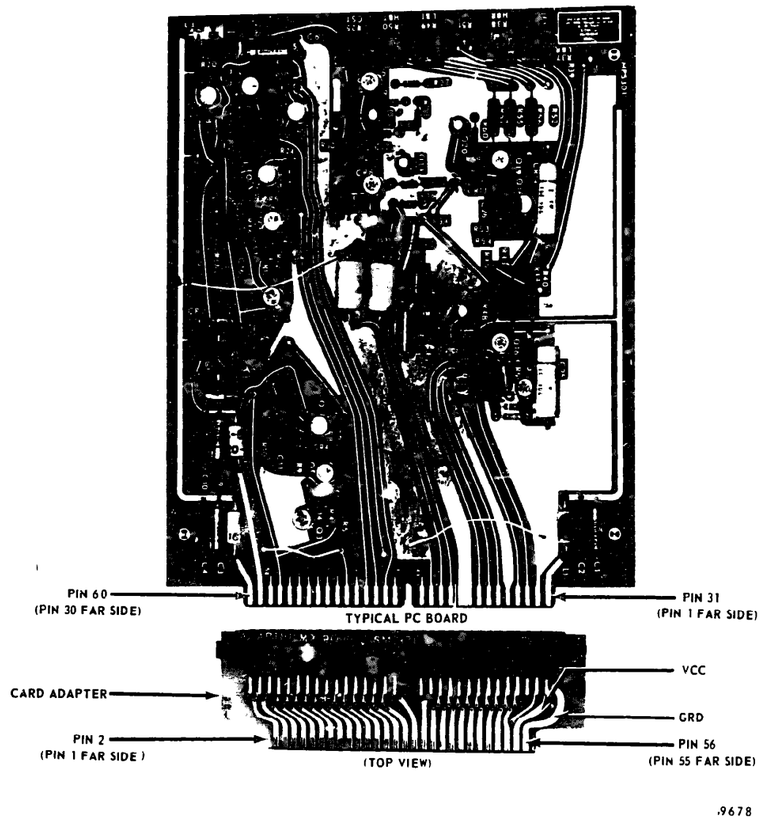


Figure 12. Printed Circuit Card Adapter MX-9095/USM-371
60 Pin TCU

Table 9. Printed Circuit Card Adapter MX-9096/USM-371
Pin Cross Reference

ADAPTER MX-9096/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9096/USM-371	CARD TESTER PIN NUMBER
*1	55	A	56 (GRD.)
*2	53	B	54 (+4.75V)
3	51	C	52
4	49	D	50
5	47	E	48
6	45	F	46
7	43	H	44
8	41	J	42
9	39	K	40
10	37	L	38
11	35	M	36
12	33	N	34
13	31	P	32
14	29	R	30
15	27	S	28
16	25	T	26
17	23	U	24
18	21	V	22
19	19	W	20
20	17	X	18
21	15	Y	16
22	13	Z	14
23	11	AA	12

* If these pins are Power/GRD they are tied to +4.5V/GRD on Autodin Card itself.

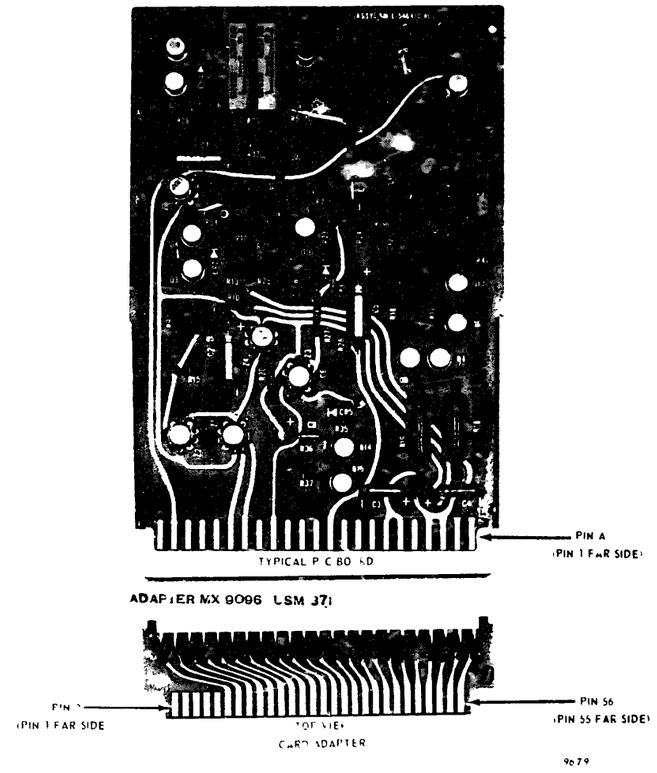


Figure 13. Printed Circuit Card Adapter MX-9096/USM-371
16 Pm GDE

Table 10. Printed Circuit Card Adapter MX-9097/USM-371
Pin Cross Reference

ADAPTER MX-9097/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9097/USM-371	CARD TESTER PIN NUMBER
1	25	13	13
2	24	14	12
3	23	15	11
4	22	16	10
5	21	17	9
6	20	18	8
7	19	19	7
8	18	20	6
9	17	21	5
10	16	22	4
11	15	23	3
1	14	24	2
		25	1

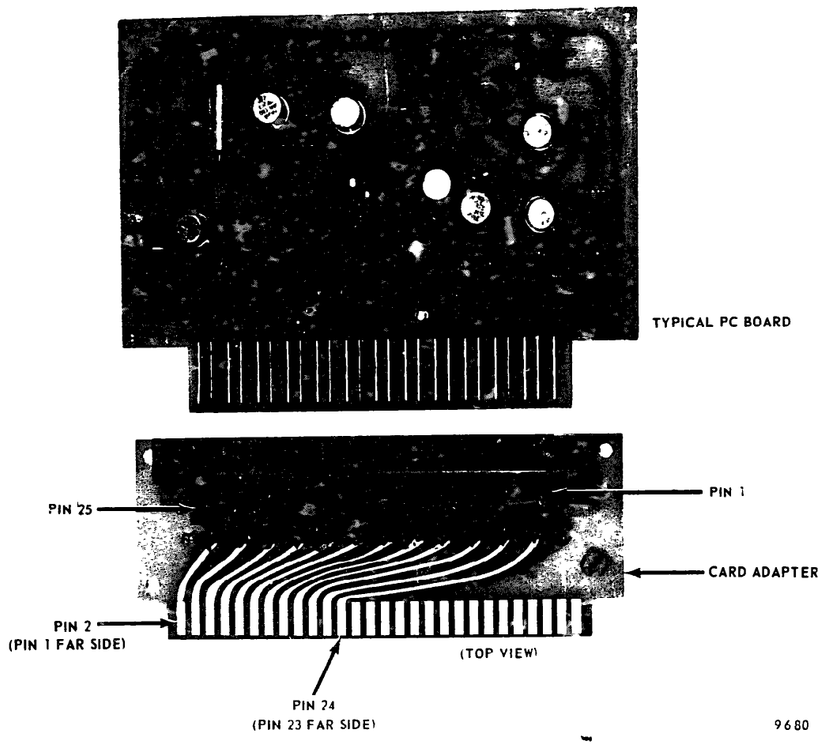
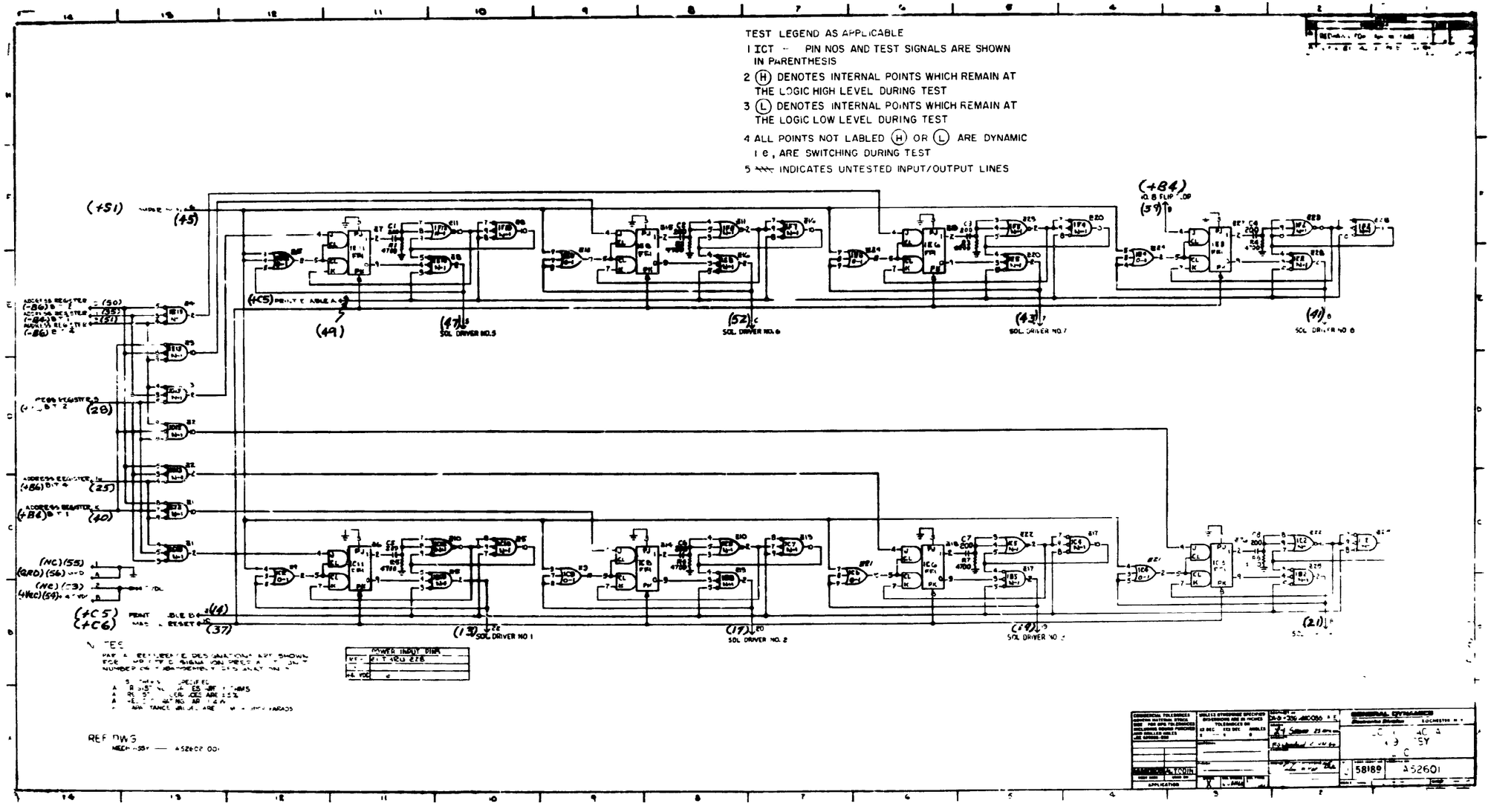


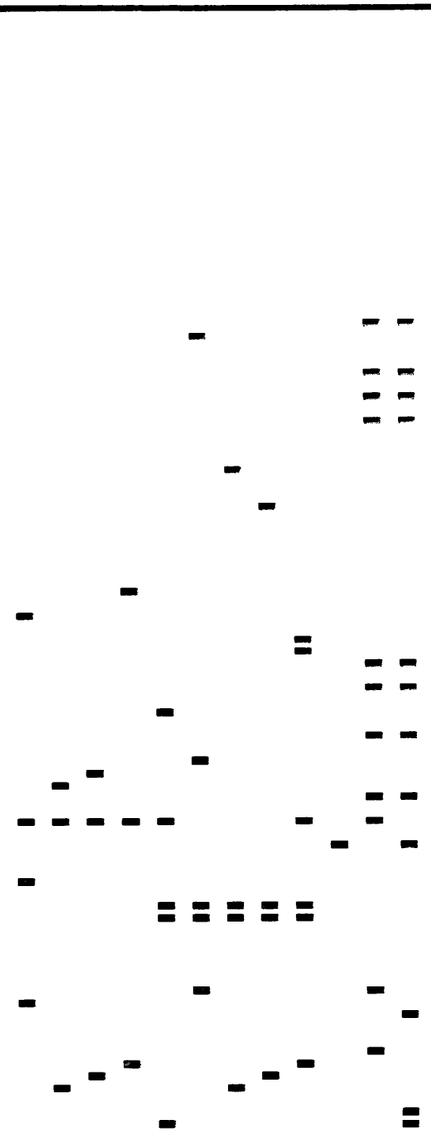
Figure 14. Printed Circuit Card Adapter MX-9097/USM-371
25 Pin FGC



7-6-71 J.N.

P.C. Assembly A52602

P.C. Logic A52601



A52602-001 DOC. NO. 23-1101-11

7-6-71 J.N

TEST PARAMETERS			
Vcc	+4.5V	SIG V	+4.5V
±V	—	LOAD REF V	GRD
+V	—	CLK	1µS
-V	—	BIT CLK	+OSC

ROW ASSIGNMENT	
10	—
1	+B4
2	+B5
3	+B6
4	+C5
5	+S1
6	-B4
7	-B5
8	-B6
9	+C6

INPUT PINS	COL	SIG
	63	+CO
	64	C1
	65	-C2
	66	-C3
	67	-C4
14, 49	68	+C5
33*	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
35* 40, 39	74	+B4
28, 50*	75	+B5
25 51*	76	+B6
	77	+B7
	78	+S0
45	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING												
13	A	1	2	3	4	5							
	B	1	7	4	10	#							
17	A	1	2	3	4	5							
	B	11	6	3	9	9							
19	A	1	2	3	4	5							
	B	10	5	2	8	#							
21	A	1	2	3	4	5							
	B	9	4	1	7	#							
47	A	1	2	3	4	5							
	B	8	3	11	6	#							
52	A	1	2	3	4	5							
	B	7	2	10	5	#							
43	A	1	2	3									
	B	6	1	#									
41	A	1	2	3	4	5	6	7	8	9	10	11	12
	B	1	7	10	5	8	3	6	1	4	10	2	8
	A												
	B												
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	A												
	B												

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.

TEST LEGEND AS APPLICABLE

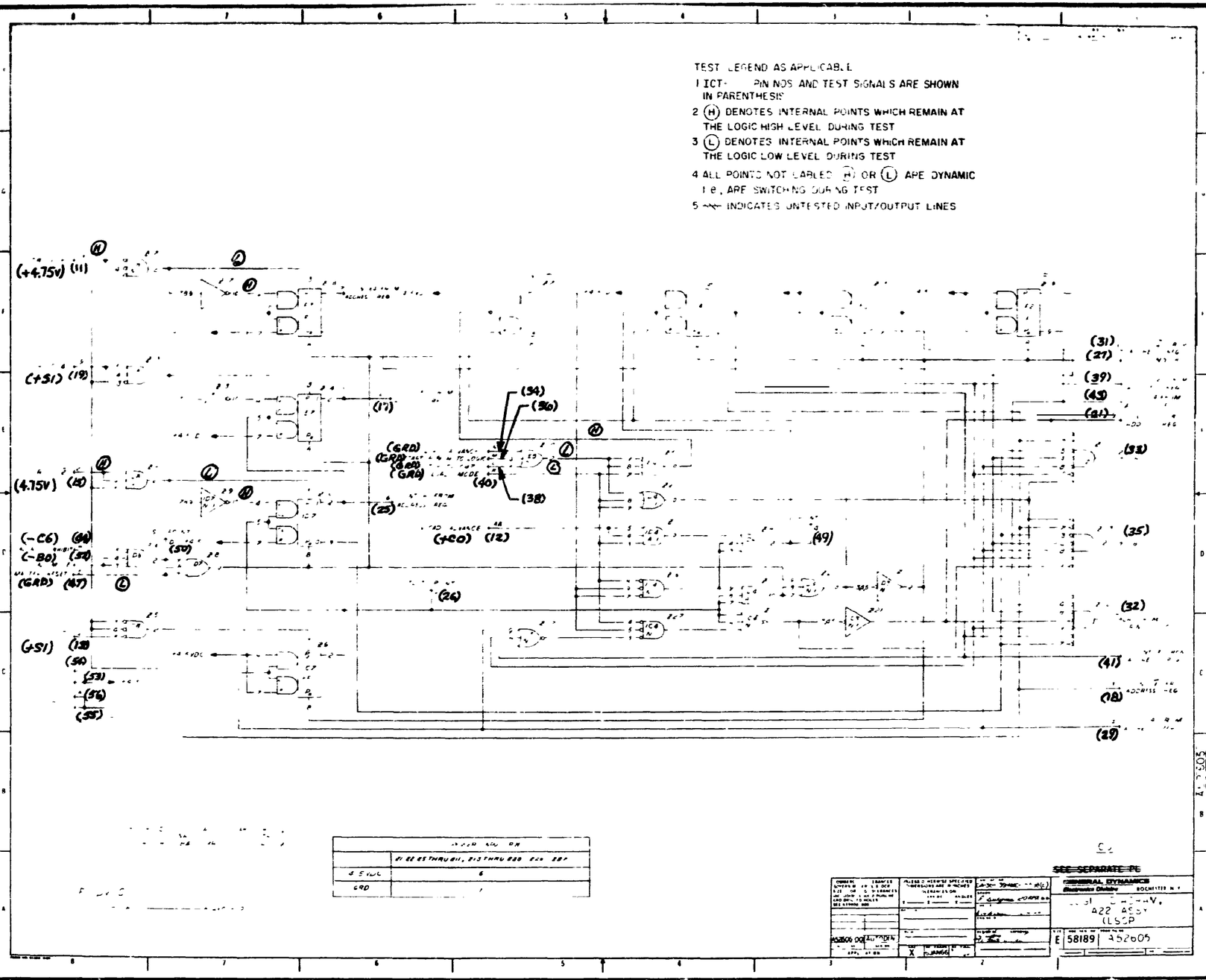
1 ICT - PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.e., ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES



	W, EE RS THRU GH, BI-S THRU BBB ECN 387
+5 VDC	6
GRD	7

SEE SEPARATE PC

GENERAL DYNAMICS
Electronics Division ROCHESTER, N.Y.

A22 ASSY (LSCP)

E 58189 A52605

7-6-71 JN

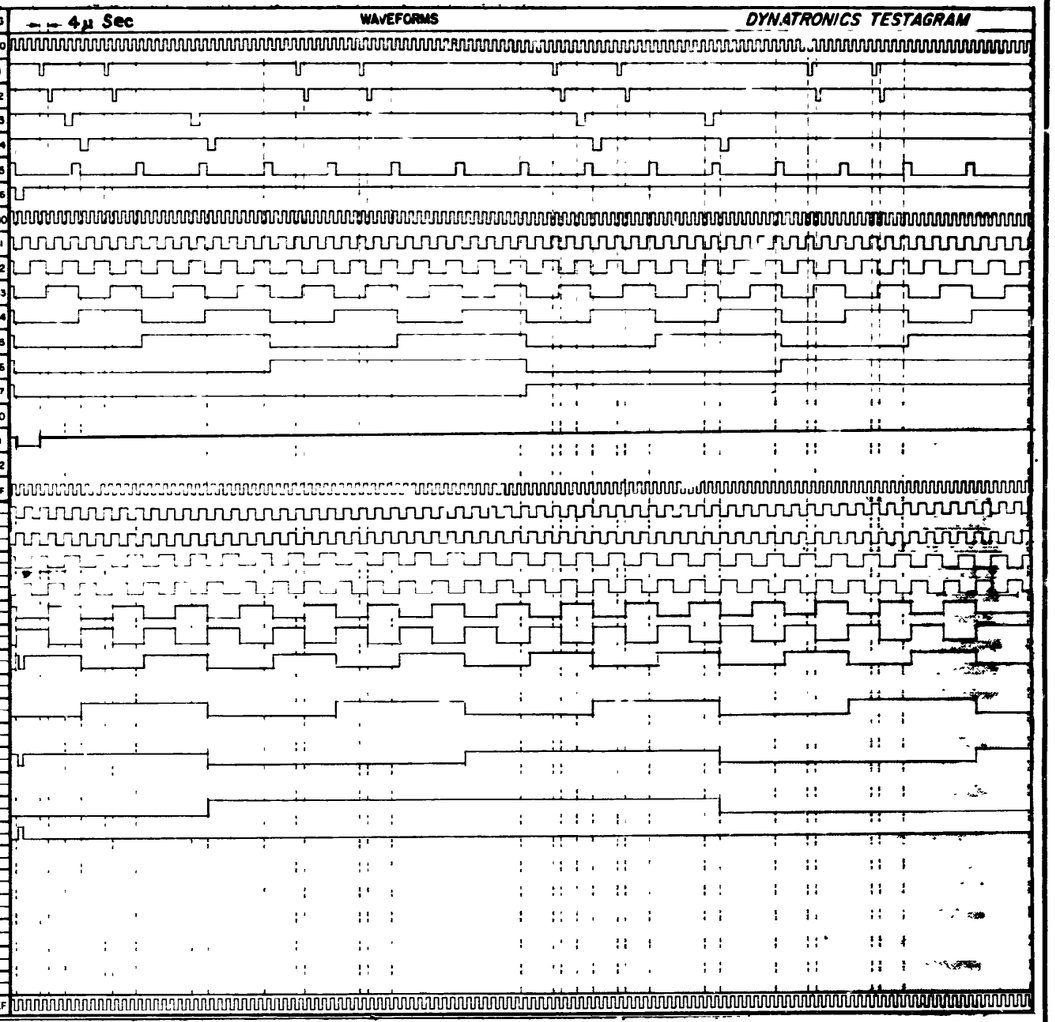
P.C. Assembly A52606-001
P.C. Logic A52605

TEST PARAMETERS			
V_{CC}	+4.75	SIG	+5V OV
±V	—	LOGIC REF V	GRD
+V	—	CLK	1 μ SEC
-V	—	REF CLK	÷ OSC

ROW ASSIGNMENT	
10	+4.75V UNDITE 21
1	-C6
2	+C0
3	+S1
4	—
5	GRD
6	-B0
7	—
8	—
9	—

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
41	A 1 2 3 / B 3 7 11
18	A 1 2 3 / B 7 11
39	A 1 2 3 / B 3 11 8
31	A 1 2 3 / B 3 11 8
29	A 1 2 3 / B 3 6 2
43	A 1 2 3 / B 3 6 2
21, 26	A 1 2 3 4 5 / B 3 4 7 2 1
25	A 1 2 3 / B 2 11 9
17	A 1 2 3 4 5 5 / B 4 7 11 7 3 10
23	A 1 2 3 / B 11 3 #
27 50	A 1 2 3 / B 4 6 #

INPUT PINS	COL	SIG
12	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
44	69	-C6
52*	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
13 19	79	+S1
	80	+S2
SWITCH SETTING	+C0 REF	



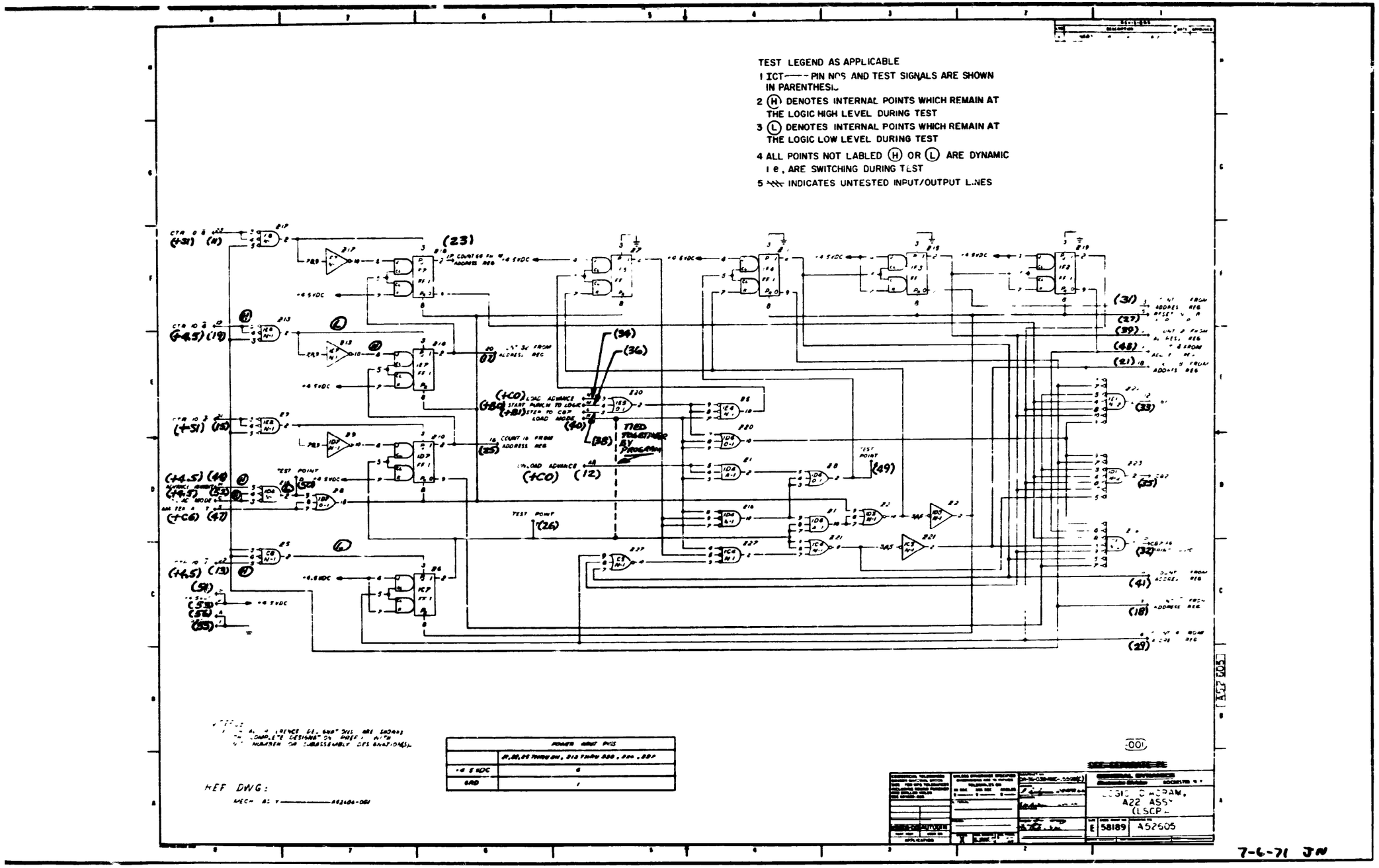
NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

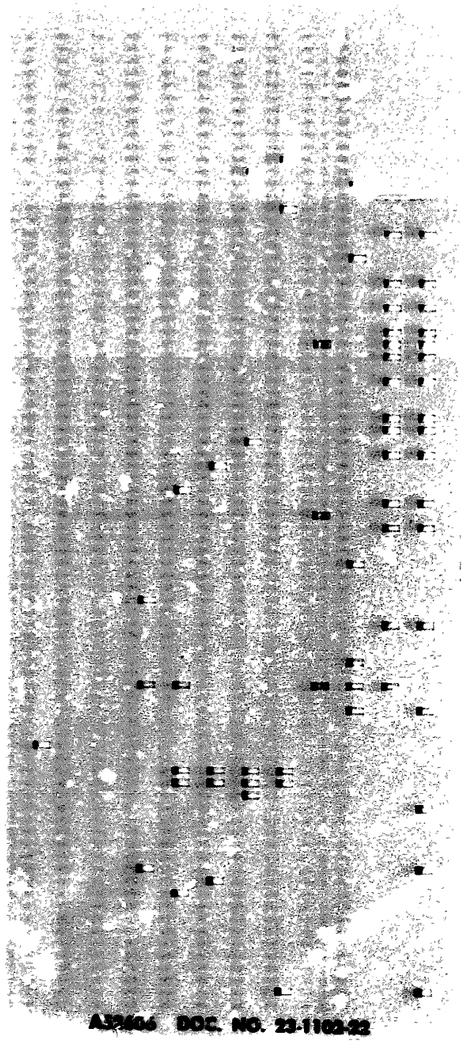
   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY AND SHOULD BE GO/NO-GO TESTED FIRST.

A52606 DOC. NO. 23 1102-12

7-6-71 JN



P.C. Assembly A52606-001
P.C. Logic A52605

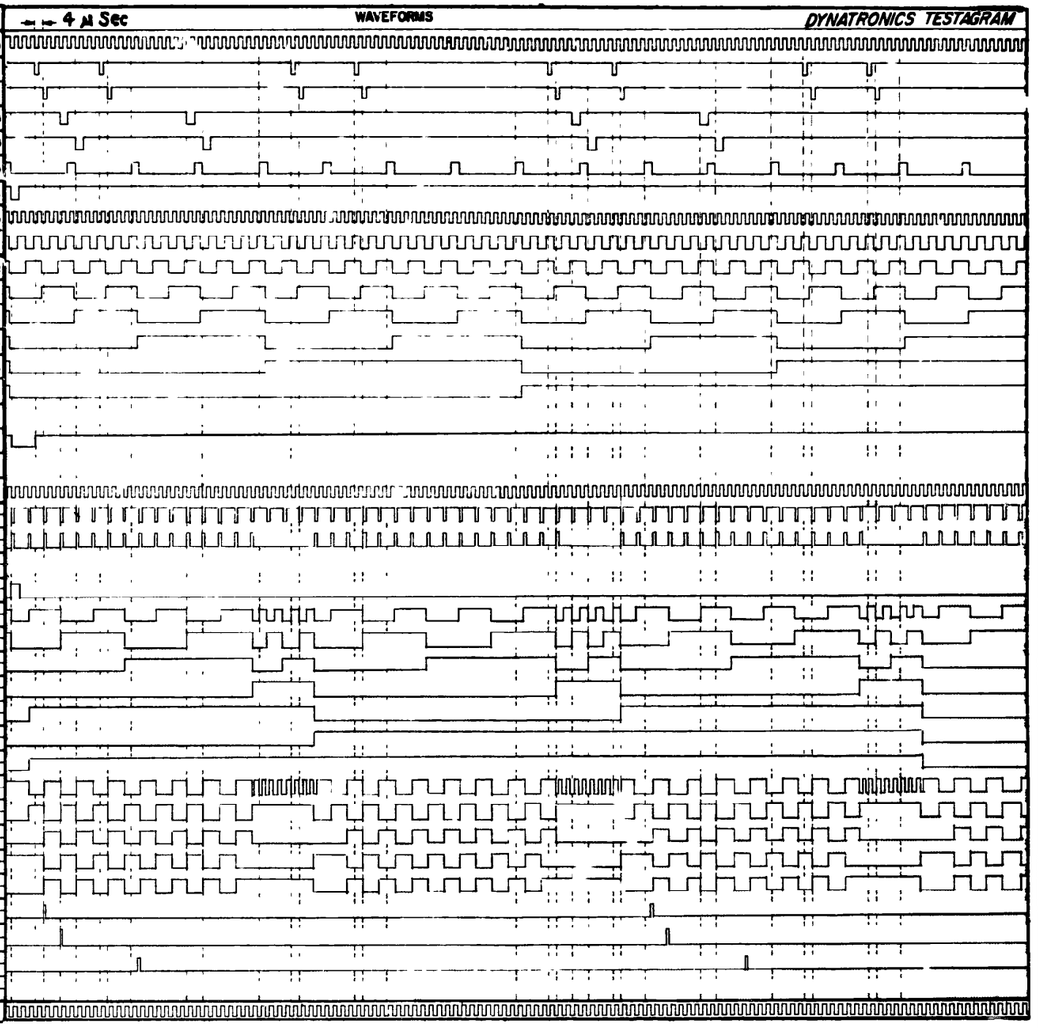


A52606 DOC. NO. 23-1102-22

TEST PARAMETERS			
V_{cc}	+4.75V	BIB REF V	1=+2V 0=0V
ΔV	—	CLOCK	GRD
ΔV	—	CLR	1 u sec
ΔV	—	INIT CLR	+OSC

ROW ASSIGNMENT	
10	+4.75V (NOTE 2)
1	COMMON BUS
2	+S1
3	+C0
4	+B0
5	+B1
6	+C6
7	—
8	—
9	—

INPUT PINS	COL	SIG
12, 34	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
47	69	-C6
36	70	+B0
38	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
11, 15	79	+S1
	80	+S2



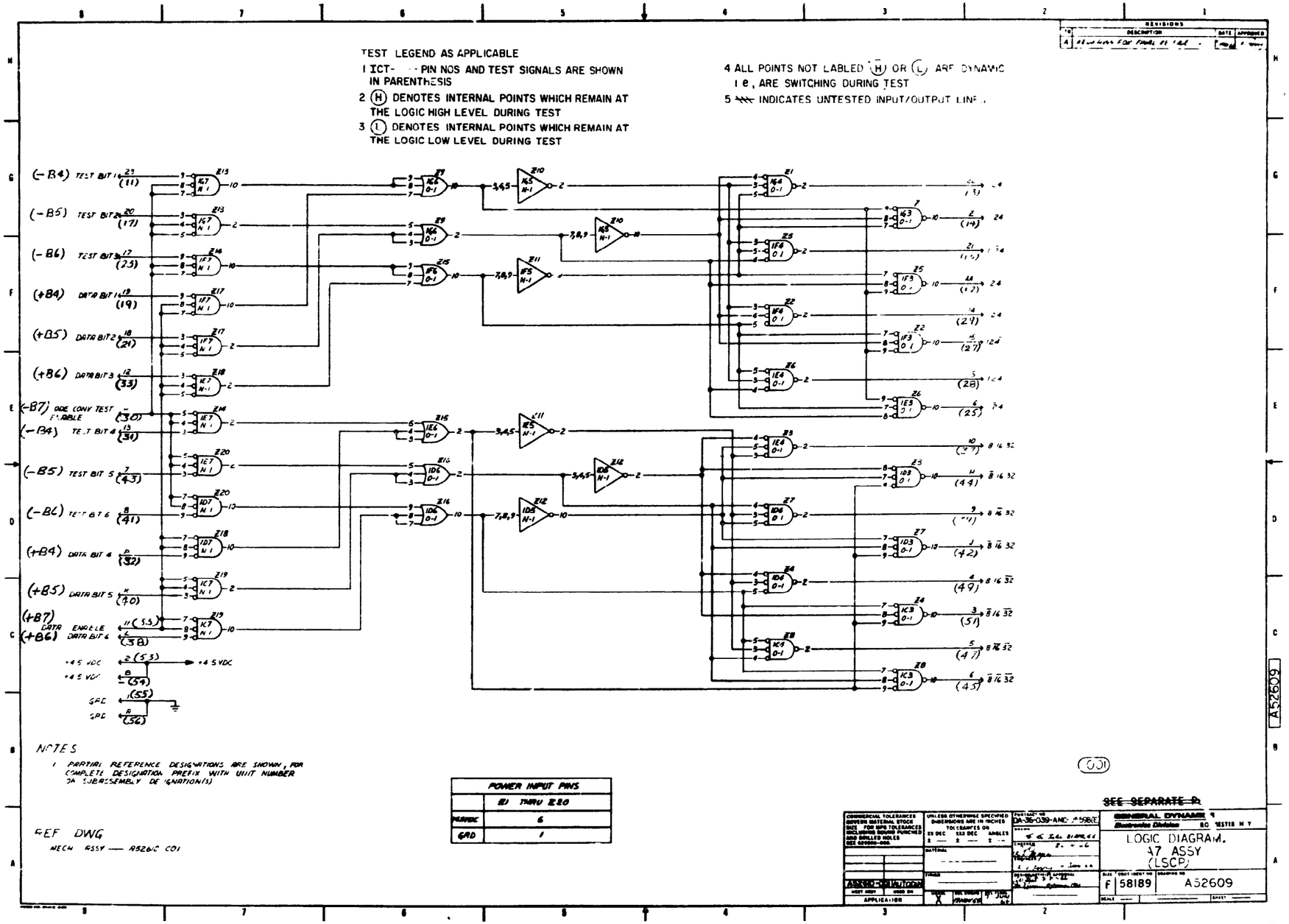
OUTPUT PINS (TEST POINTS)	SWITCH SETTING	+C0 REF
Z20-2	A B	
Z5-10	A B	
	A B	
27	A 1 2 3 / B 3 7 #	
41	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 3 1 6 11 5 1* 4 9 3 6 10 3	
39	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 3 6 # 4 3 10 7 4 1 4 3 2	
29	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 5 3 7 1 3 1 5 10 1 10 3 8	
26	A 1 2 3 4 5 6 7 / B 3 1 1 10 10 8 #	
25	A 1 2 3 4 5 / B 1 1 10 8 #	
17	A 1 2 3 / B 1 8 #	
23	A 1 2 3 / B 1 8 #	
49	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 1 9 6 3 11 8 5 2 10 7 4 1	
Z7-2	A B	
Z27-2	A B	
Z21-10	A B	
21	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 3 9 6 3 11 8 5 2 10 7 4 1	
33	A 1 2 3 4 5 / B 8 9 4 5 #	
35	A 1 2 3 4 5 / B 5 6 1 2 #	
32	A 1 2 3 4 5 / B 1 2 8 9 #	
	A B	

NOTES:

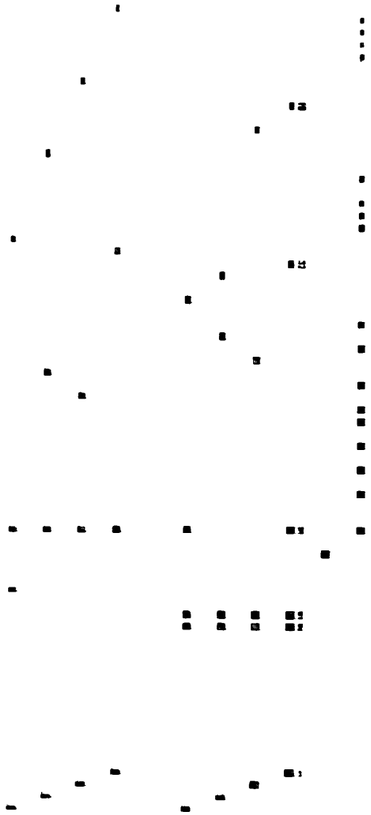
1. ASTERISK INDICATES SIGNAL INVERTED BY PROGRAMMING.
2. +4.75V ON PINS 13,19,44,52.
3. PINS 26 AND 40 TIED TOGETHER BY TEST PROGRAM.
4. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.

7-6-71 JN


TEST LEGEND AS APPLICABLE
1 ICT- -- PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST
5 INDICATES UNTESTED INPUT/OUTPUT LINE
(-B4) TEST BIT 1
(-B5) TEST BIT 2
(-B6) TEST BIT 3
(+B4) DATA BIT 1
(+B5) DATA BIT 2
(+B6) DATA BIT 3
(-B7) ODE CONV TEST ENABLE
(-B4) TEST BIT 4
(-B5) TEST BIT 5
(-B6) TEST BIT 6
(+B4) DATA BIT 4
(+B5) DATA BIT 5
(+B7) DATA ENABLE
(+B6) DATA BIT 6
+4.5 VDC
+4.5 VDC
GND
GND
NOTES
1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OF SUBASSEMBLY DESIGNATION(S)
REF DWG
MECH ASSY — A52610 C01
POWER INPUT PINS
ALL THRU Z80
+5 VOLTS 6
GND 1
SEE SEPARATE P.
GENERAL DYNAMICS
Electronics Division
ROCHESTER N.Y.
LOGIC DIAGRAM.
A7 ASSY
(LSCP)
F 58189
A52609
A52609

7-6-71 JN



A52610-001 DOC. NO. 23-1103-11

TEST PARAMETERS			
Vcc	+4.75	SIG GND	GND / VCC
±V	—	LOAD REF V	11, VCC
+V	—	CLK	2 µ SEC
-V	—	INT CLK	OSC

ROW ASSIGNMENT	
10	—
1	+B4
2	+B5
3	+B6
4	+B7
5	—
6	-B4
7	-B5
8	-B6
9	B7

INPUT PINS	COL.	SIG
	63	+C0
	64	C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
19 32 14* 31*	74	+B4
21 40 17* 43*	75	+B5
33 38 22* 41*	76	+B6
35 30*	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
13 37	A 1 2 / B 1 9
14 44	A 1 2 3 4 / B 1 11 10 9
15 39	A 1 2 3 4 / B 11 12 11 10
12 42	A 1 2 3 4 / B 10 9 1 11
29 49	A 1 2 3 4 / B 9 8 2 1
27 51	A 1 2 3 4 / B 8 7 3 2
28, 47	A 1 2 3 4 / B 7 6 4 3
25 45	A 1 2 / B 6 4
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B

8 µsec WAVEFORMS DYNATRONICS TESTAGRAM

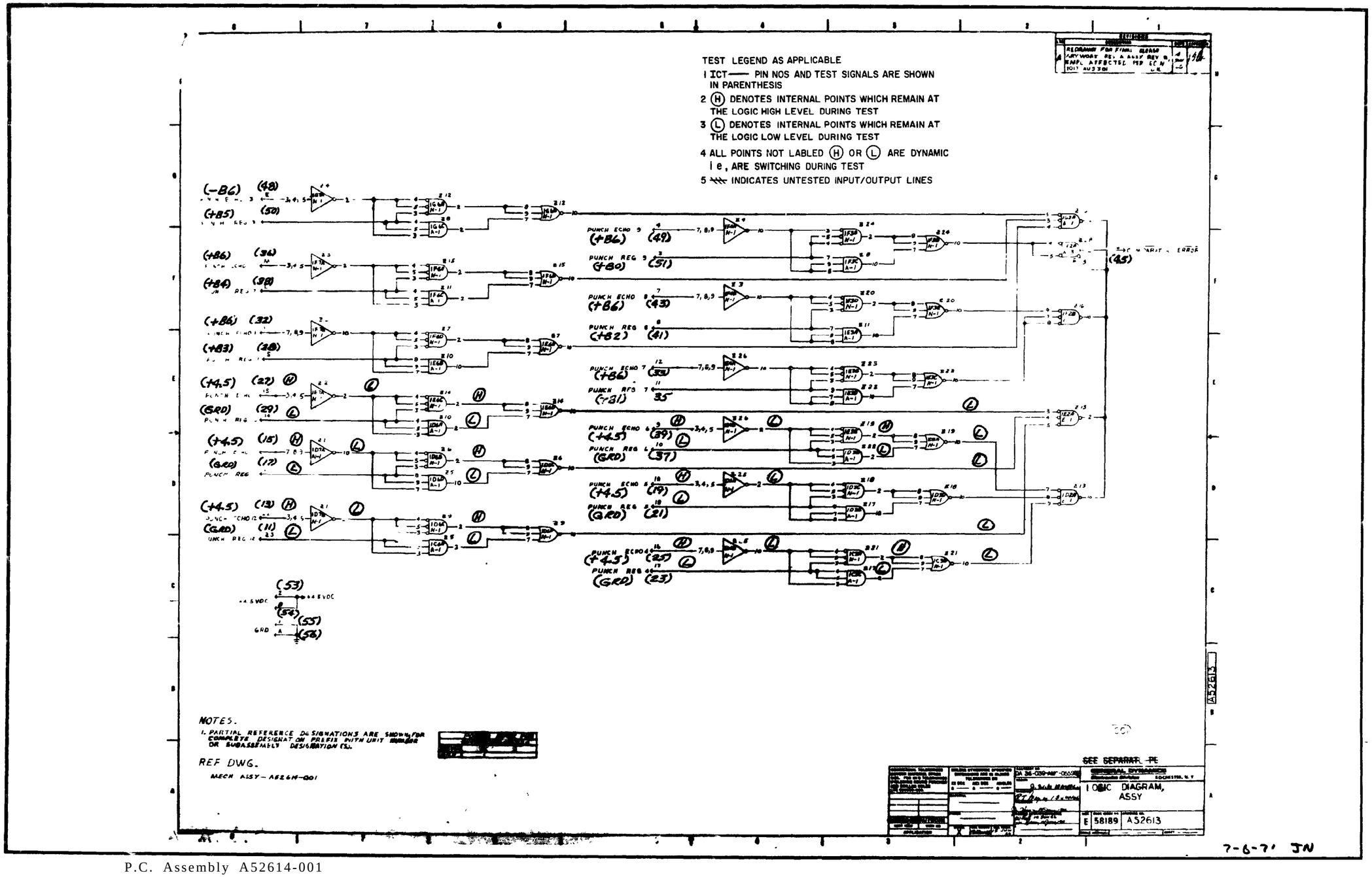
+C0 REF

+B0 REF

NOTES:

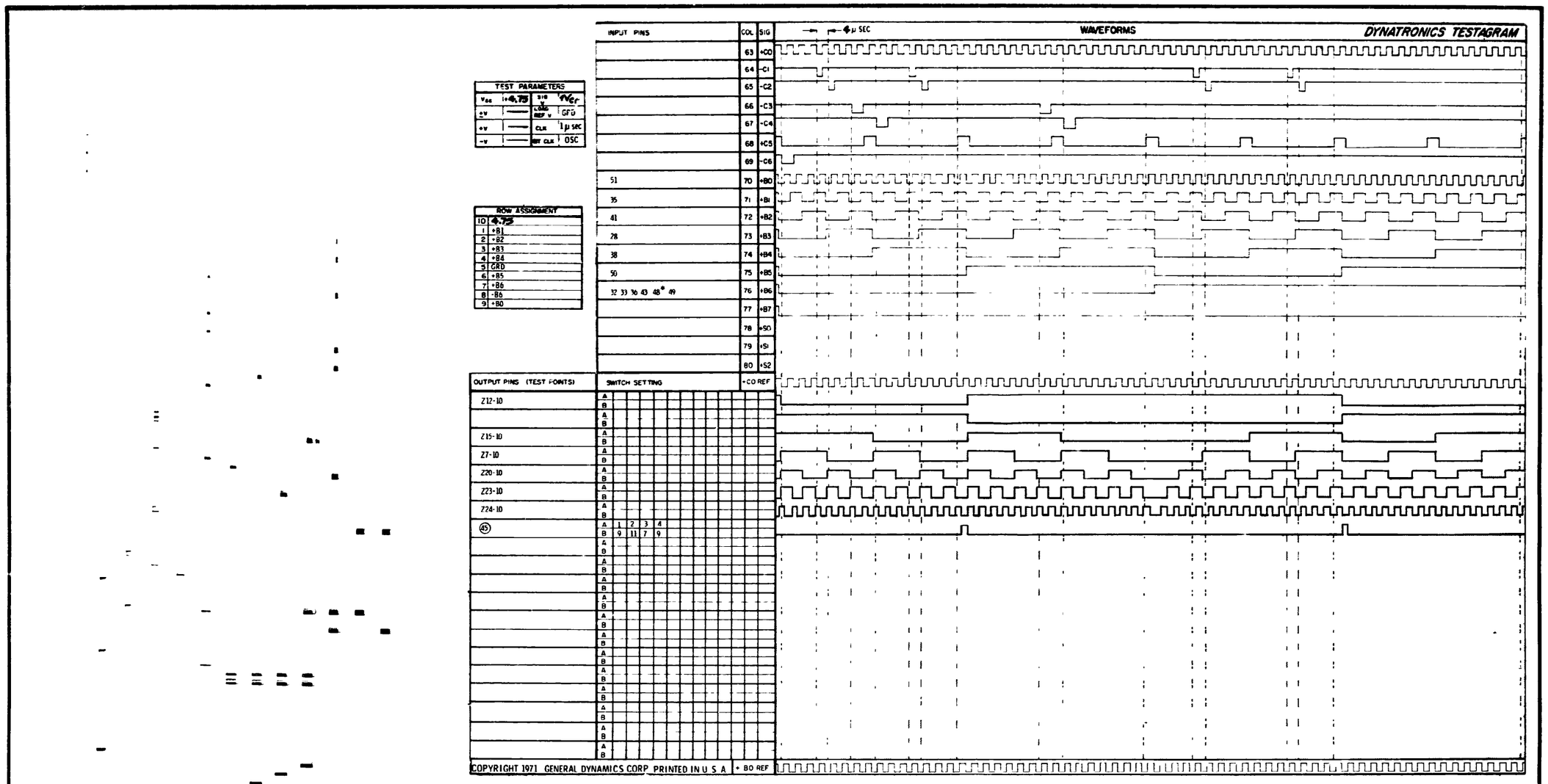
1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

7-6-71 JN



P.C. Assembly A52614-001

P.C. Logic A52613

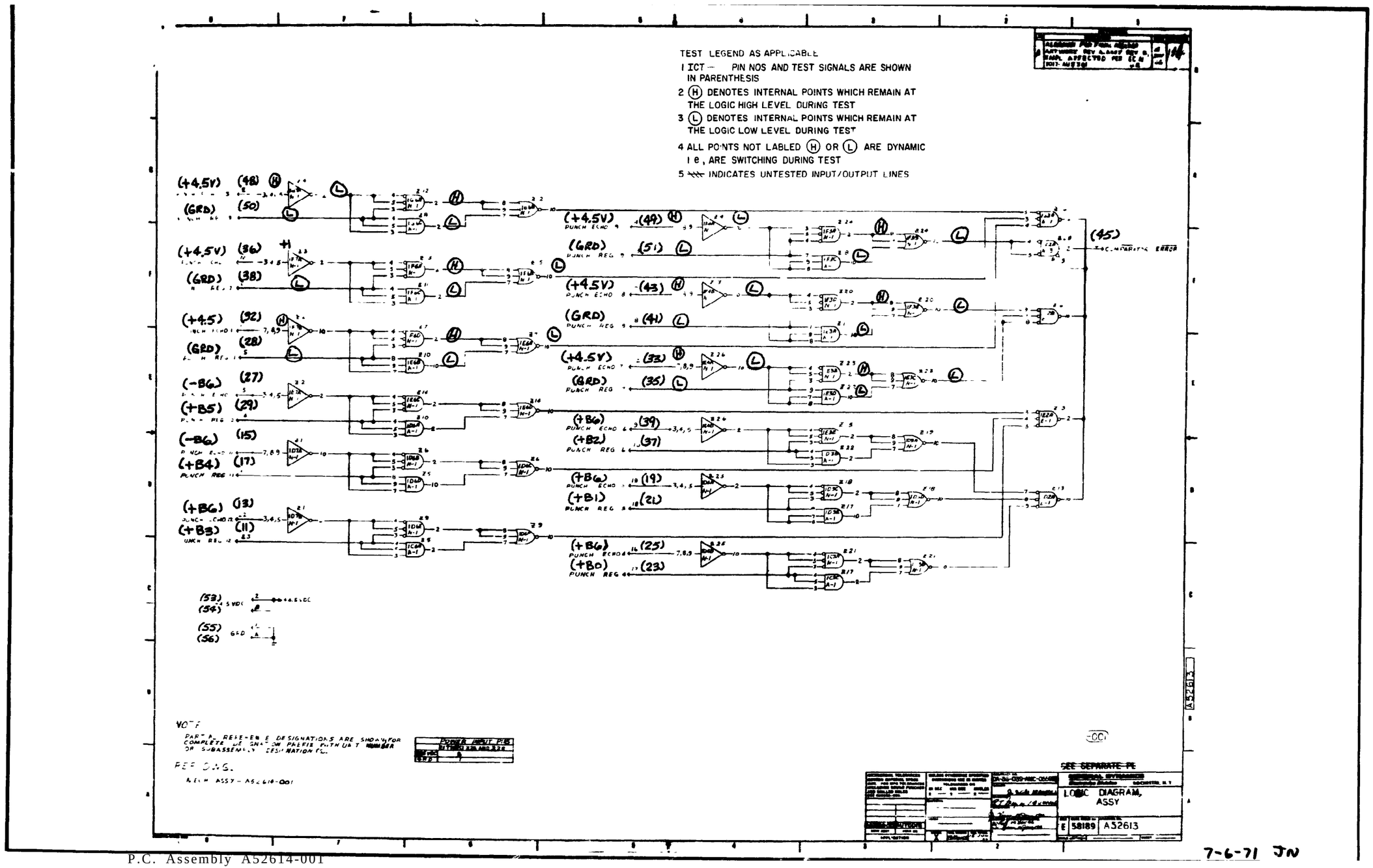


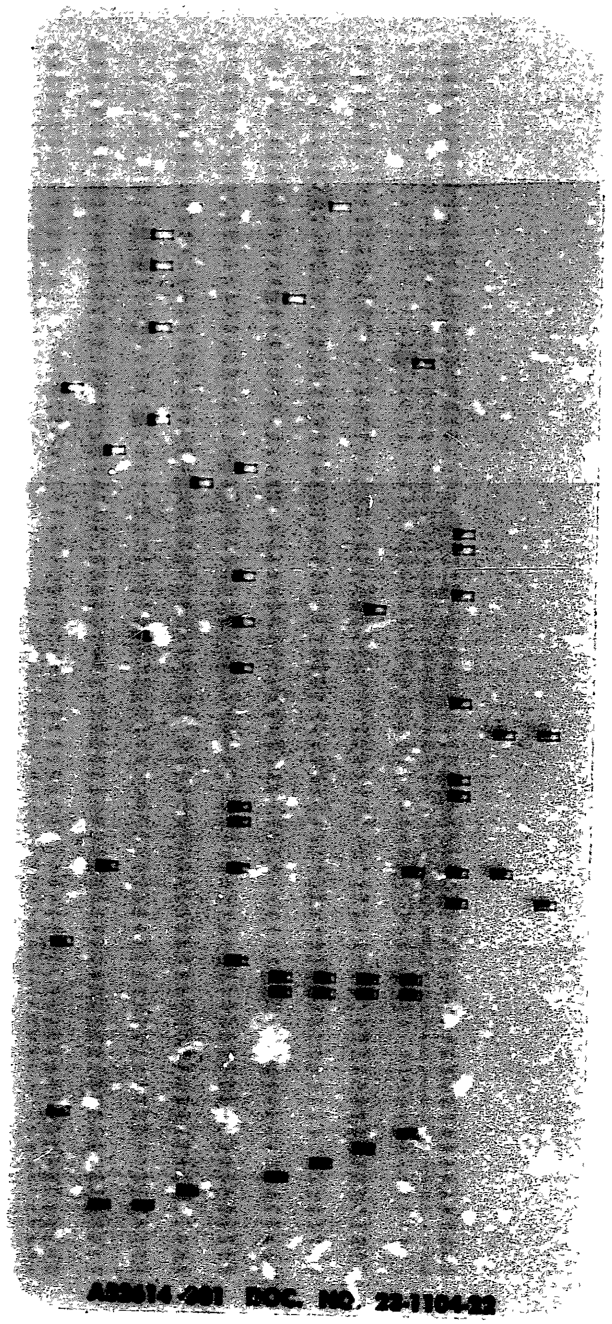
A52614 DOC. NO. 23-1104-12

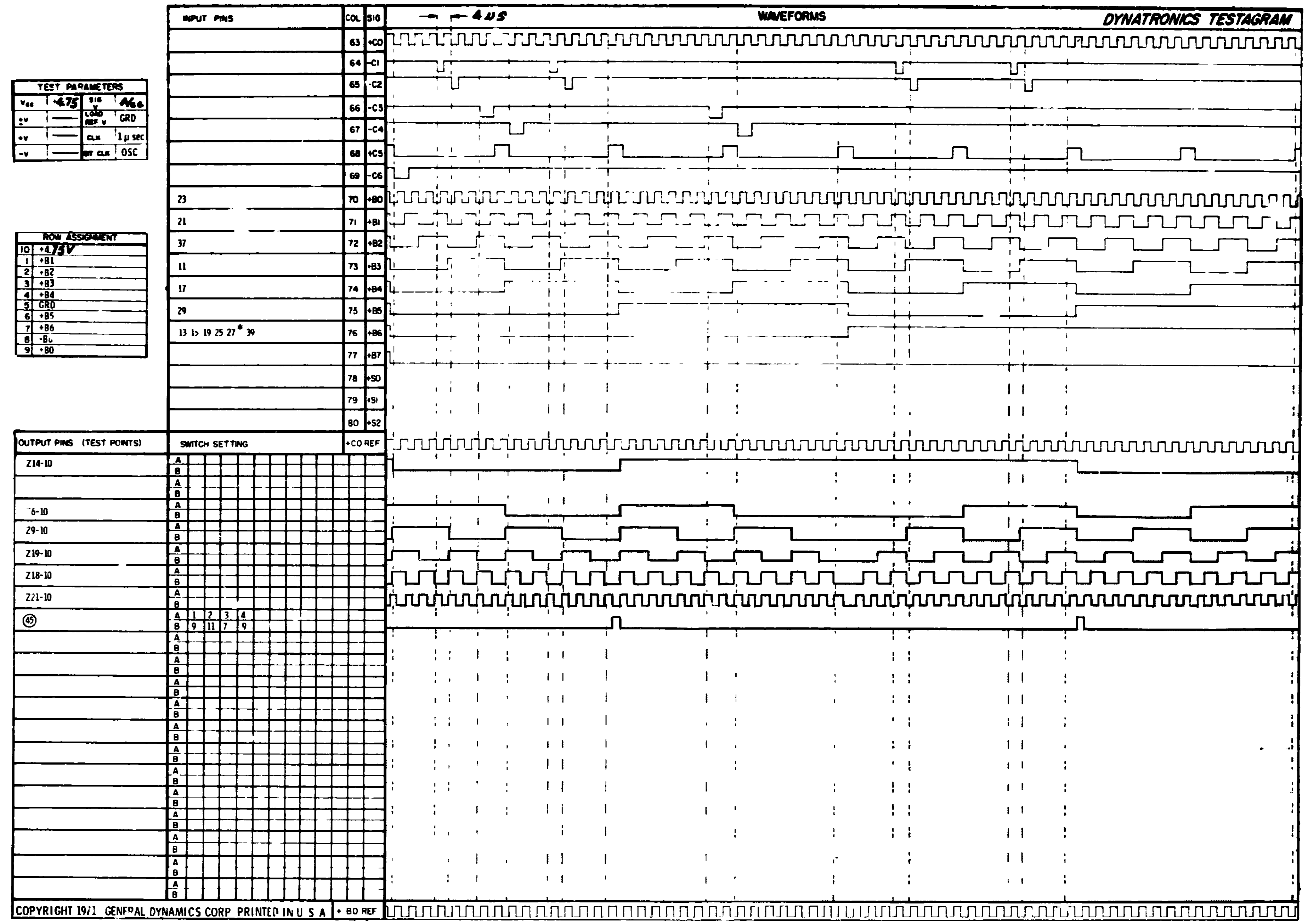
NOTES:

1. *DENOTES INVERTED INPUT.
2. VCC (+5 EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. PINS 11,17,21,23,29 & 37 TIED TO GROUND.
5. PINS 13,15,19,25,27 & 39 TIED TO +4.75VDC.

7-6-71 JN


TEST LEGEND AS APPLICABLE
1 ICT — PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST
5 INDICATES UNTESTED INPUT/OUTPUT LINES
(+4.5V)
(GRD)
(-BG)
(+B5)
(+B4)
(+BG)
(+B3)
(+B6)
(+B2)
(+B0)
(+B1)
(45)
(53)
(54)
(55)
(56)
5 VDC
GRD
NOTE
PART A REFERENCE DESIGNATORS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OF SUBASSEMBLY DESIGNATION FOR
REF DWG.
ASSY - A52614-001
POWER INPUT PIN
SEE SEPARATE PE
LOGIC DIAGRAM, ASSY
E 58189 A52613
A52613
-001
7-6-71 JN

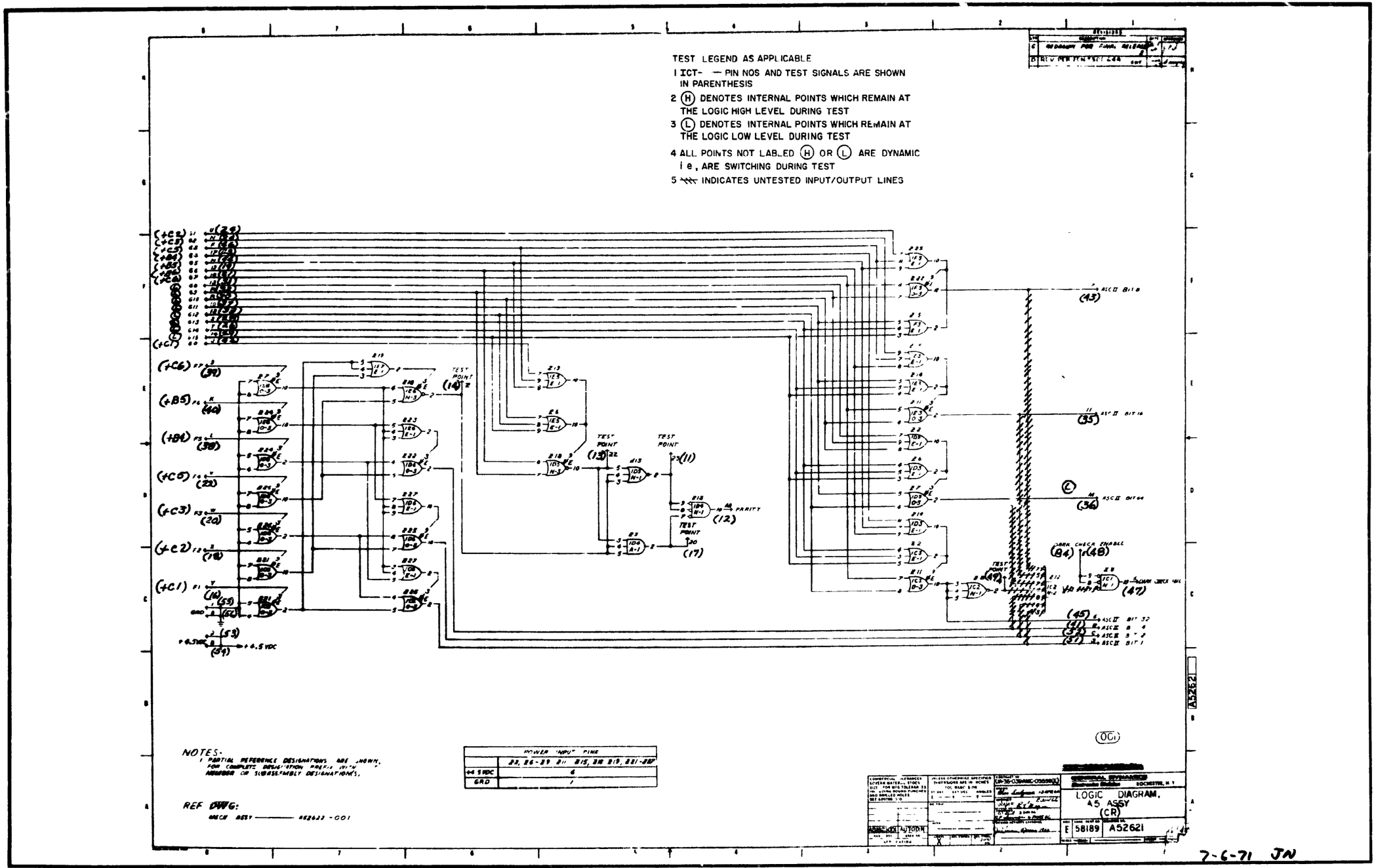




NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5 EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. PINS 28,35,38,41,50 & 51 ARE TIED TO GROUND.
5. PINS 32,3 36,43,48 & 49 ARE TIED TO +4.75VDC.

7-6-71 JN



P.C. Assembly A52622-001

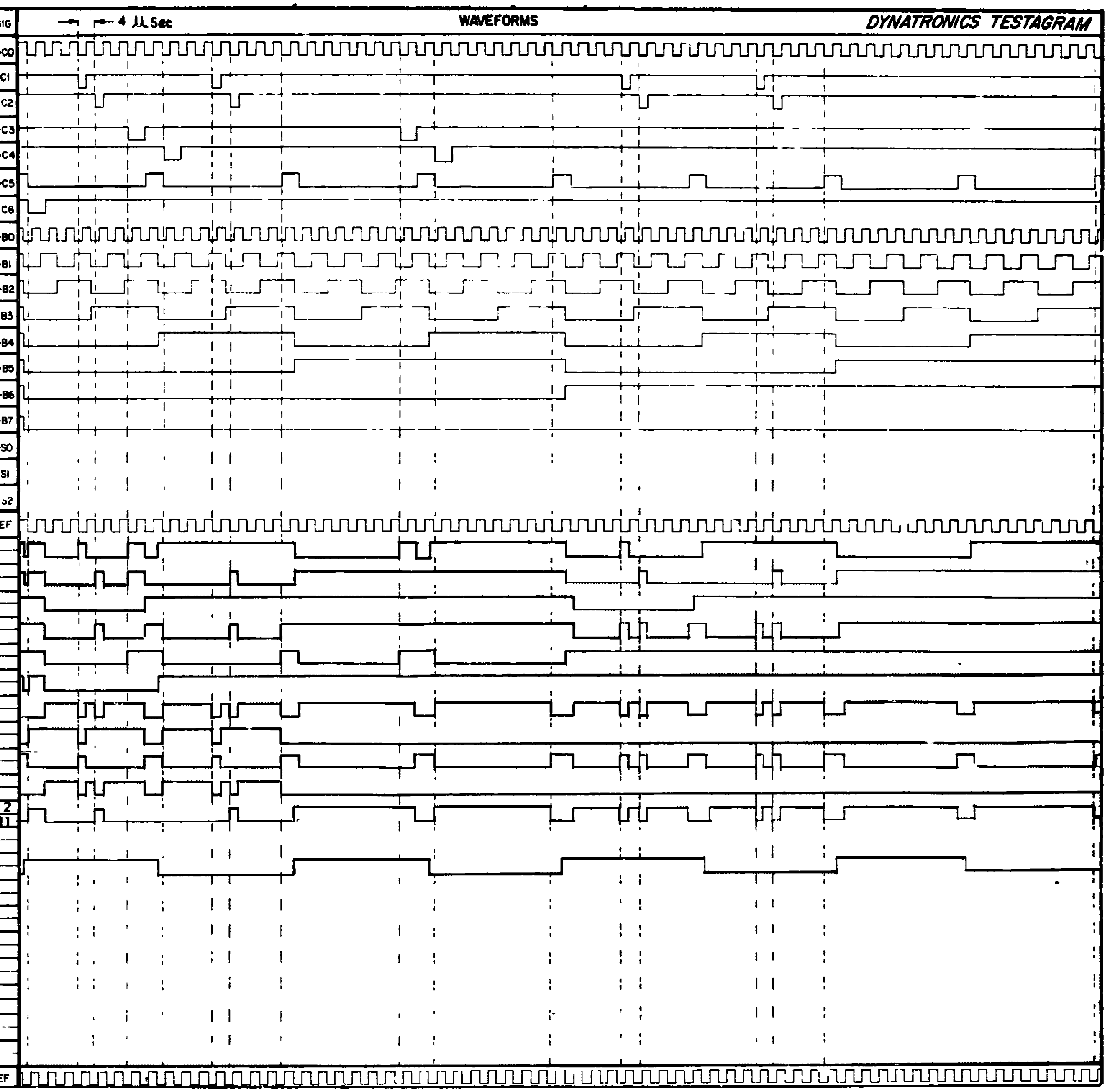
P.C. Logic A52621

TEST PARAMETERS			
+Vcc	4 75	SIG V	+Vcc
±V	——	LOAD REF V	GND
+V	——	CLK	1 μsec
-V	——	BIT CLK	+OSC

ROW ASSIGNMENT	
10	—
1	—
2	B6
3	B5
4	B4
5	C5
6	C1
7	C2
8	C3
9	C6

INPUT PINS	COL	SIG
	63	+C0
16* 42*	64	-C1
18* 24*	65	-C2
20* 34*	66	-C3
	67	-C4
22 46	68	+C5
39* 21*	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
38 23 48	74	+B4
40 44	75	+B5
19	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING												
(51)	A	1	2	3	4	5	6	7	8	9			
	B	2	3	7	4	6	5	9	1	11			
(52)	A	1	2	3	4	5	6	7	8	9	10	11	
	B	2	3	7	8	10	5	9	7	9	11	9	
(41)	A	1	2	3	4	5	6	7	8				
	B	7	9	10	5	6	1	2	8				
43	A	1	2	3	4	5	6	7	8	9			
	B	7	8	10	9	2	7	9	8	10			
35	A	1	2	3	4	5	6	7	8				
	B	7	5	2	8	[illegible]	3	11	6				
(45) 49*	A	1	2	3	4	5	6	7					
	B	2	3	7	1	5	4	#					
14	A	1	2	3	4	5	6	7	8	9			
	B	7	4	6	8	10	9	2	3	5			
13	A	1	2	3	4	5	6	7	8	9			
	B	3	4	6	9	2	3	5	8	6			
11	A	1	2	3	4	5							
	B	3	4	6	9	2							
17	A	1	2	3	4	5	6	7	8				
	B	7	4	6	8	10	9	2	3				
(12)	A	1	2	3	4	5	6	7	8	9	10	11	12
	B	3	7	8	10	7	9	1	7	11	6	10	11
	A												
	B												
47	A	1	2										
	B	2	1										



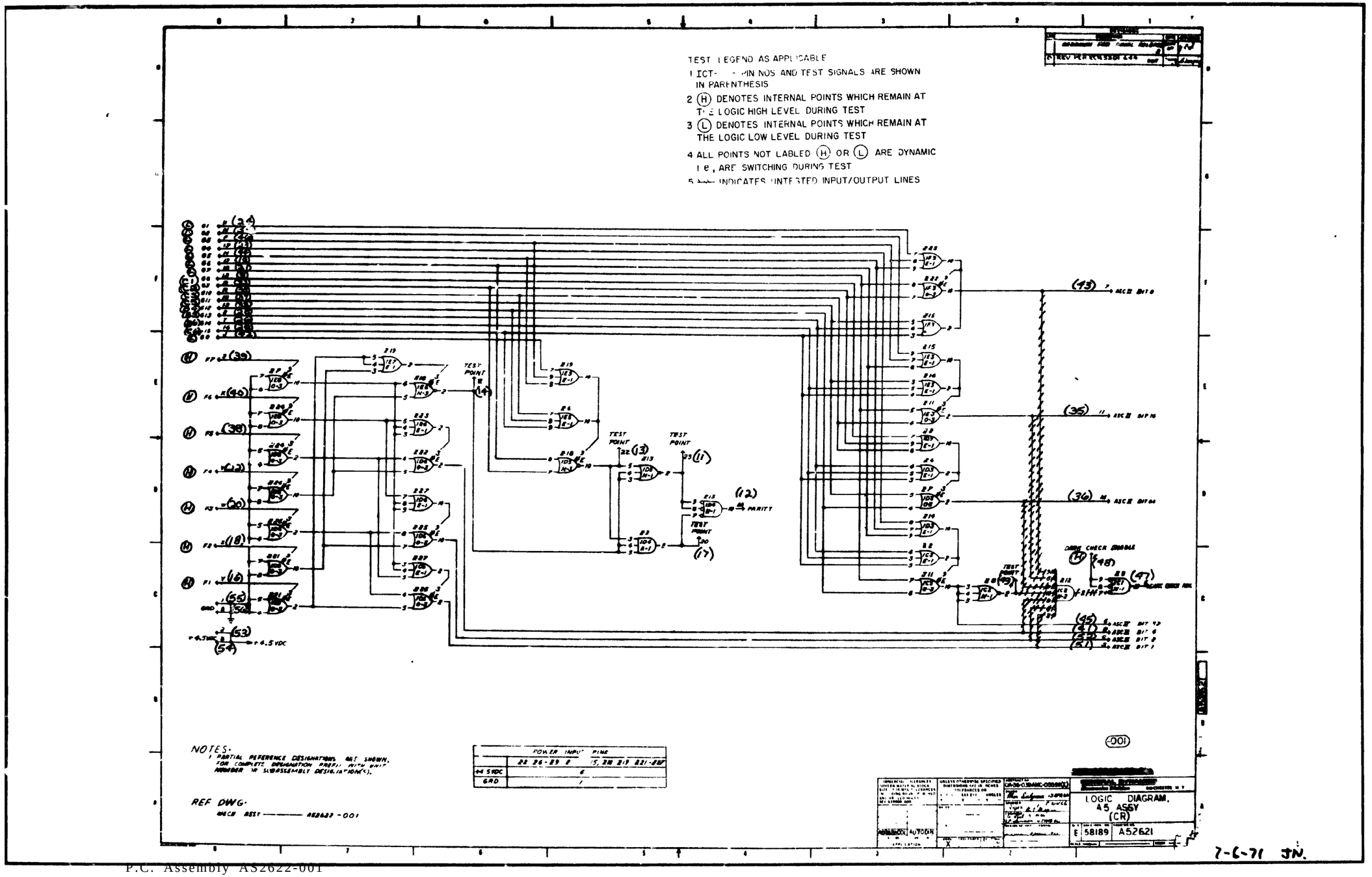
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

A52622-001 DOC. NO. 23-1105-12

7-6-71 JN



P.C. Assembly A52622-001

P.C. Logic A52621

TEST PARAMETERS			
+V_{cc}	4.75	SIG GEN REF. V	0_2+VCC
0V	—	GND	GND
+V	—	CLK	1_{μ} SEC
-V	—	WT CLK	+OSC

ROW ASSIGNMENT	
10	—
1	—
2	B6
3	B5
4	B4
5	C5
6	C1
7	C2
8	C3
9	C6

INPUT PINS	COL	SIG
	63	+CO
31*	64	-C1
32*	65	-C2
30*	66	-C3
	67	-C4
37	68	+C5
29*	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
33	74	+B4
28	75	+B5
26	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

WAVEFORMS — 4 μS — DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
43	A 1 2 3 4 5 6 7 / B 7 8 10 9 2 7 9
35	A 1 2 3 4 5 6 7 8 9 / B 7 5 2 8 1 3 11 6 ¢
45	A 1 2 3 4 5 / B 2 3 7 1 5
36	A 1 2 3 4 5 6 7 / B 7 4 6 8 10 5 6
	A / B
(13)	A 1 2 3 4 5 6 7 8 9 / B 2 3 7 8 10 5 9 1 11
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B

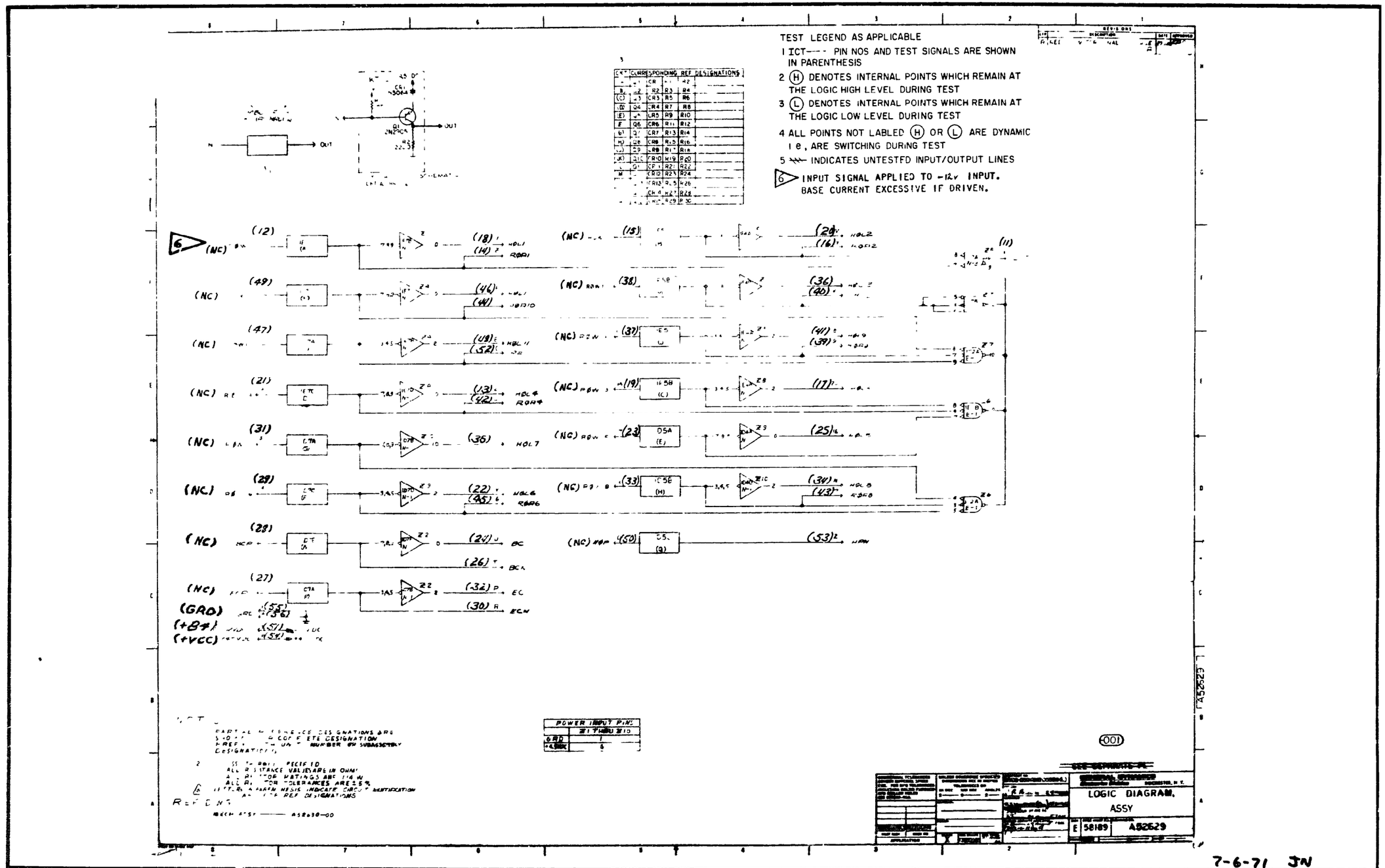
+CO REF

 + 80 REF

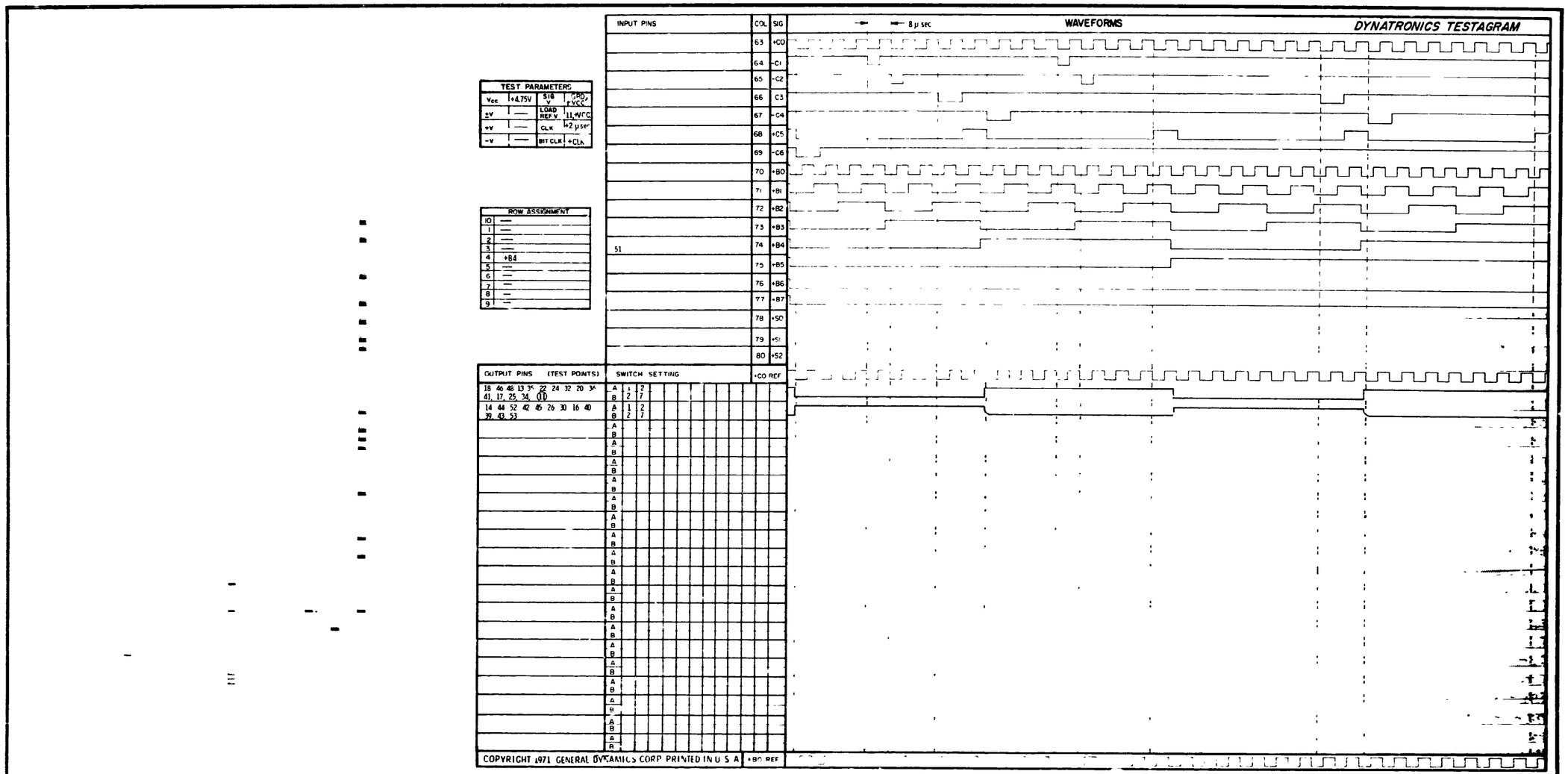
NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

7-6-71 JW



P.C. Assembly A52631

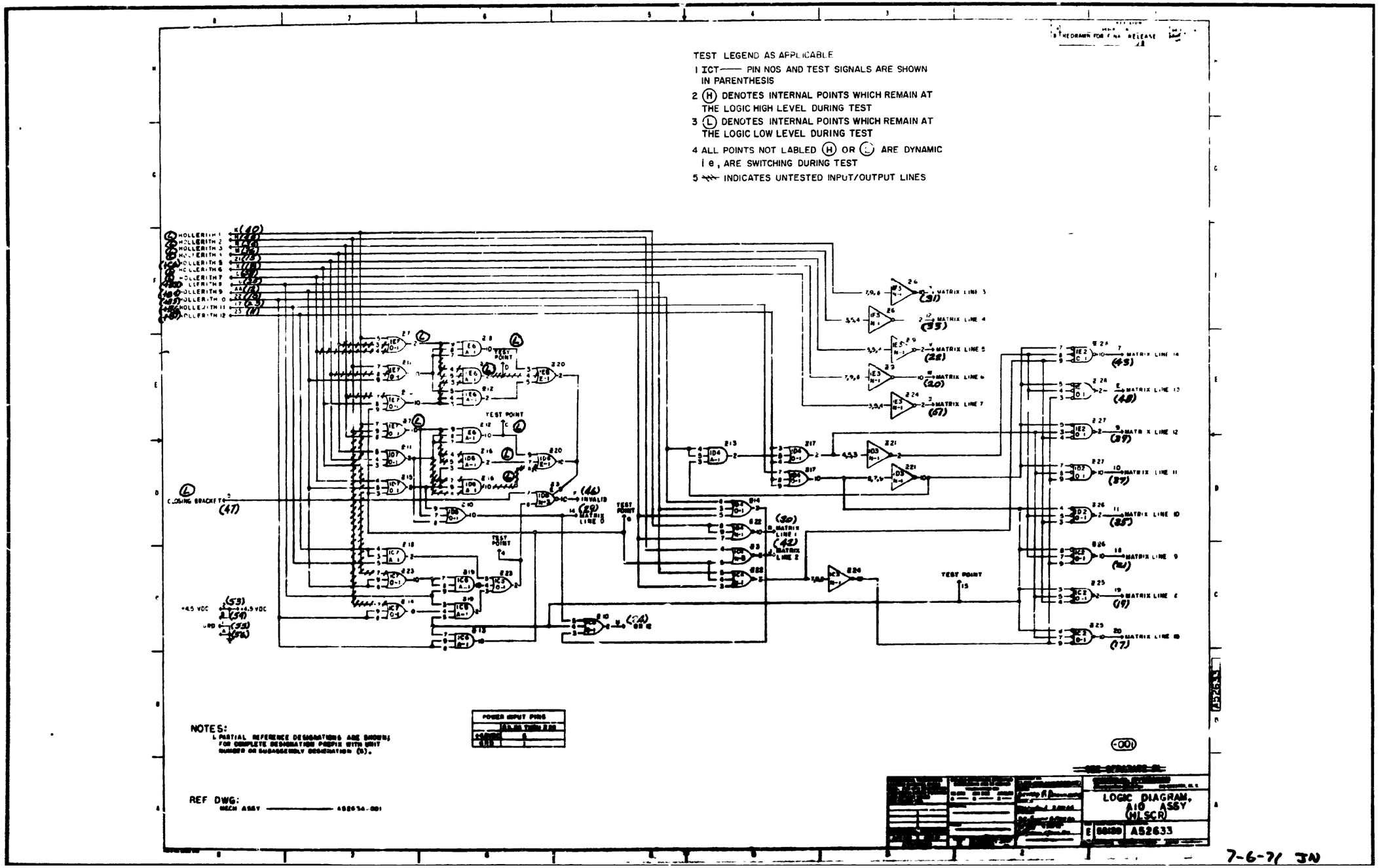


NOTE:

1. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

A52630-001 DOC. NO. 23-1105-11

7-6-71 JN



P. C. Assembly A52634-001

P. C. Logic A52633

TEST PARAMETERS

Vcc	+4.75V	S	+VCC GND
±V		AD	12GND
+V		CLK	1 μSEC
-V		BIT CLK	-OSC

ROW ASSIGNMENT

10	+B3
1	+B4
2	+B5
3	+B7
4	
5	
6	-C6
7	
8	
9	

INPUT PINS	COL	SIG
	63	-C0
	64	C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
15*	69	-C6
	70	+B0
	71	+B1
	72	+B2
75	73	+B3
12	74	+B4
13	75	+B5
73	76	+B6
11	77	+B7
	78	+S0
	79	+S1
	80	+S2
SWITCH SETTING		+CO REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
29	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 2 3 7 1 11 10 9 8 5 4 1 11
(20)	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 2 6 11 4 9 2 7 1 5 9 3 #
30	A 1 2 3 4 / B 2 1 11 10
32	A 1 2 3 4 5 6 7 / B 2 7 5 3 1 10 #
(45)	A 1 2 3 4 5 / B 2 10 1 6 #
(48)	A 1 2 3 4 5 / B 5 10 1 6 #
(39)	A 1 2 3 / B 3 2 #
(37)	A 1 2 3 / B 9 3 #
(35)	A 1 2 3 / B 5 9 #
(21)	A 1 2 3 / B 11 5 #
(19)	A 1 2 3 / B 7 11 #
(17)	A 1 2 3 / B 2 7 #
27	A 1 2 3 / B 3 7 #
24	A 1 2 4 5 / B 2 3 7 7 #
	A B
	A B
	A B
	A B
	A B
	A B
	A B

WAVEFORMS — 4μ SEC — DYNATRONICS TESTAGRAM

NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

A52634-001 DOC. NO. 23-1107-12

7-6-71 JN

TEST LEGEND AS APPLICABLE

1 ICT—— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

5 ⋙ INDICATES UNTESTED INPUT/OUTPUT LINES

NOTES:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S).

REF DWG

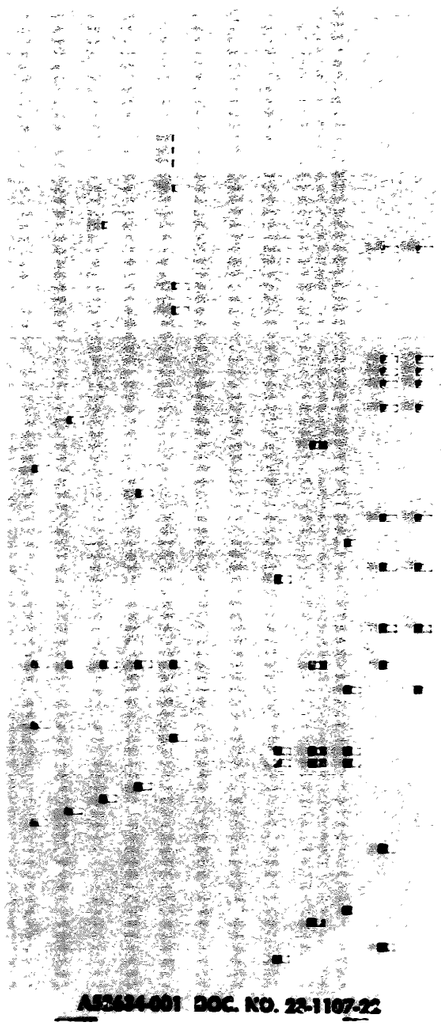
MECH ASSY ——— 52634-001

POWER INPUT PINS	
	23-28 THRU 22
+5VDC	6
GND	1

LOGIC DIAGRAM, AIO ASSY (HLSCR)

58189 A52E33

7-6-71 JN



A52634-001 DOC. NO. 23-1107-22

TEST PARAMETERS			
+Vcc	+4.75V	816	+Vcc, SIG.
-V	——	LOAD REF V	12 GRD 11 Vcc
+V	——	CLK	1 μ Sec
-V	——	SHF CLK	+OSC

ROW ASSIGNMENT	
10	+R4
1	+B5
2	+S0
3	—
4	—
5	GRD
6	+C1
7	+C2
8	+C3
9	+C4

INPUT PINS	COL	SIG
	63	+00
40*	64	-1
18*	65	-C2
34*	66	-C3
38*	67	-C4
	68	+C5
	69	-C6
	70	+80
	71	+81
	72	+82
	73	+83
44	74	+84
36	75	+85
	76	+86
	77	+87
47	78	+S0
	79	+S1
	80	+S2
		+GO REF

WAVEFORMS — 4 μ Sec

DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
(46)	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 2 3 7 2 6 3 5 7 9 3 7 10
31	A 1 2 3 4 / B 5 9 3 7
33	A 1 2 3 / B 2 11 9
20	A 1 2 3 4 / B 8 10 7 9
51	A 1 2 3 4 / B 2 6 11 4
(29)	A 1 2 3 4 5 6 7 8 ^ / B 2 4 6 8 10 5 9 1 9
30	A 1 2 3 4 / B 4 6 3 5
42	A 1 2 3 / B 2 1 11
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B

 • 80 REF

NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "±" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

7-6-71 JN

TEST LEGEND AS APPLICABLE

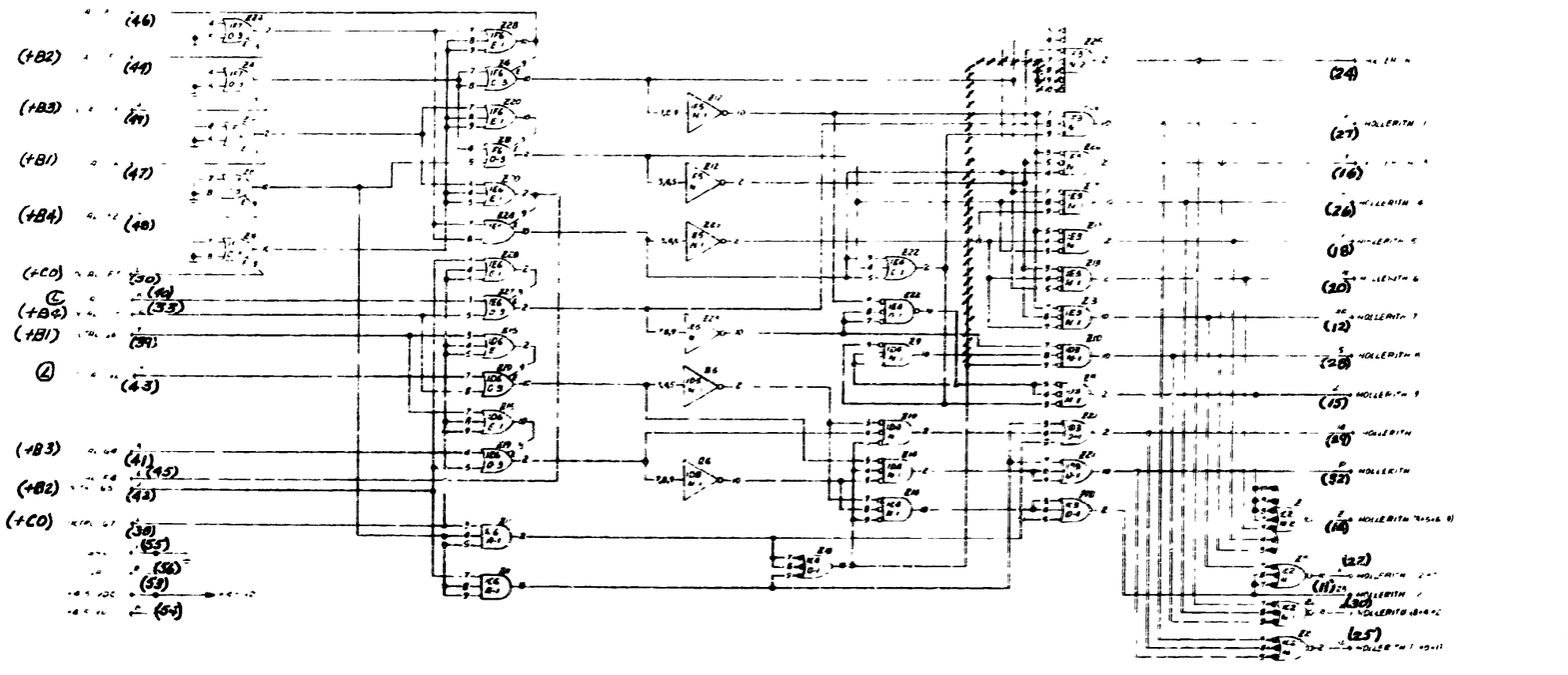
1 ICT- - PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES



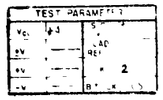
P.C. Assembly A52638-001

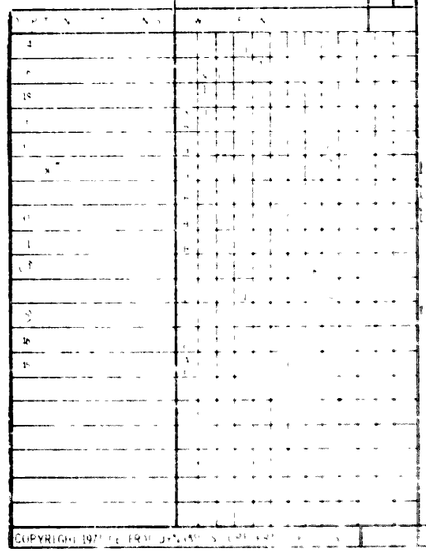
4 2 P.C. Logic A52637

WAVEFORMS

DYNATRONICS TESTAGRAM

TEST PARAMETERS





NOTES

1. * DENOTES [illegible]
2. VCC (5.0V) [illegible] ±.25V.
3. [illegible] SHOULD BE [illegible]

A52638-001 DOC. NO. 23-1103-12

7-6-71 JN

TEST LEGEND AS APPLICABLE

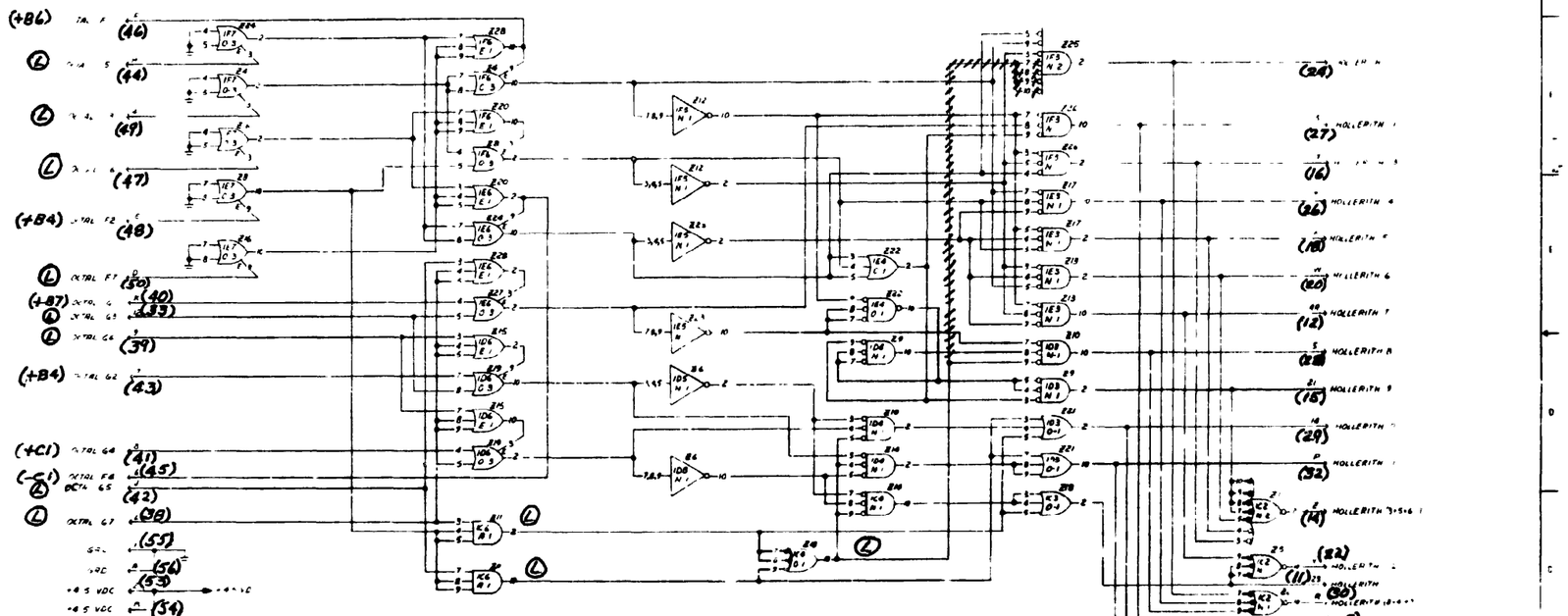
1 ICT—— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i e , ARE SWITCHING DURING TEST

5 ≈ INDICATES UNTESTED INPUT/OUTPUT LINES



NOTES

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

REF DWG

POWER INPUT PINS	
	E7, E8, E9, E10, E11, E12 PIN 8
GND	7
+4.5 VDC	6

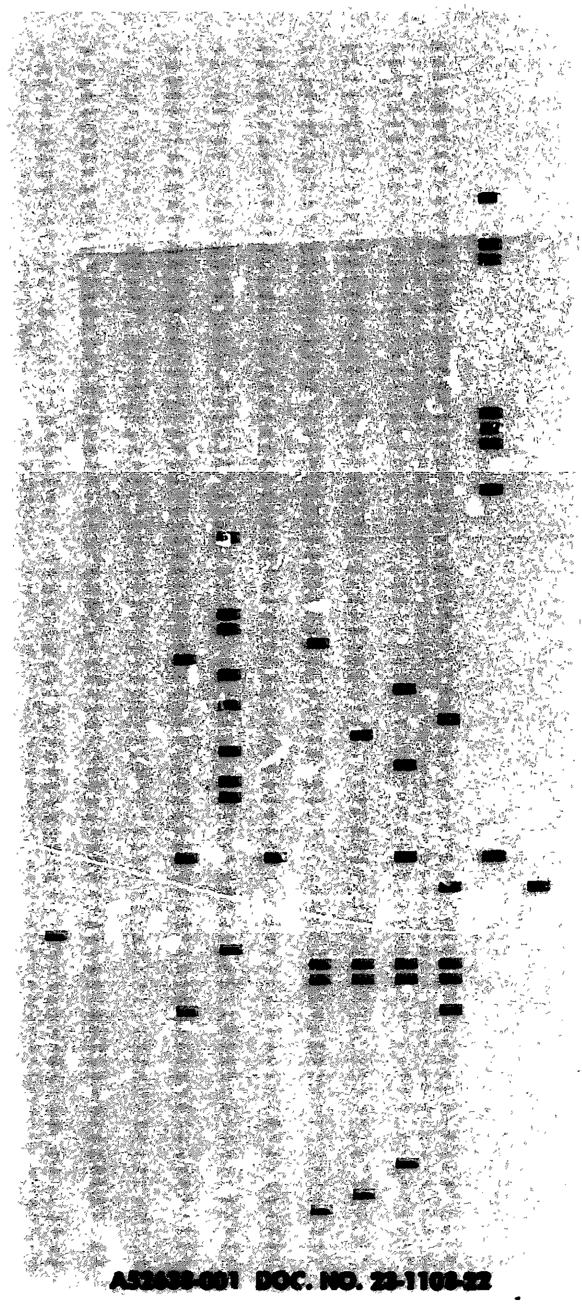
LOGIC DIAGRAM, A12 ASSY (LSCP)

E 58189 A52637

7-6-71 JN

P.C. Assembly A52638-001

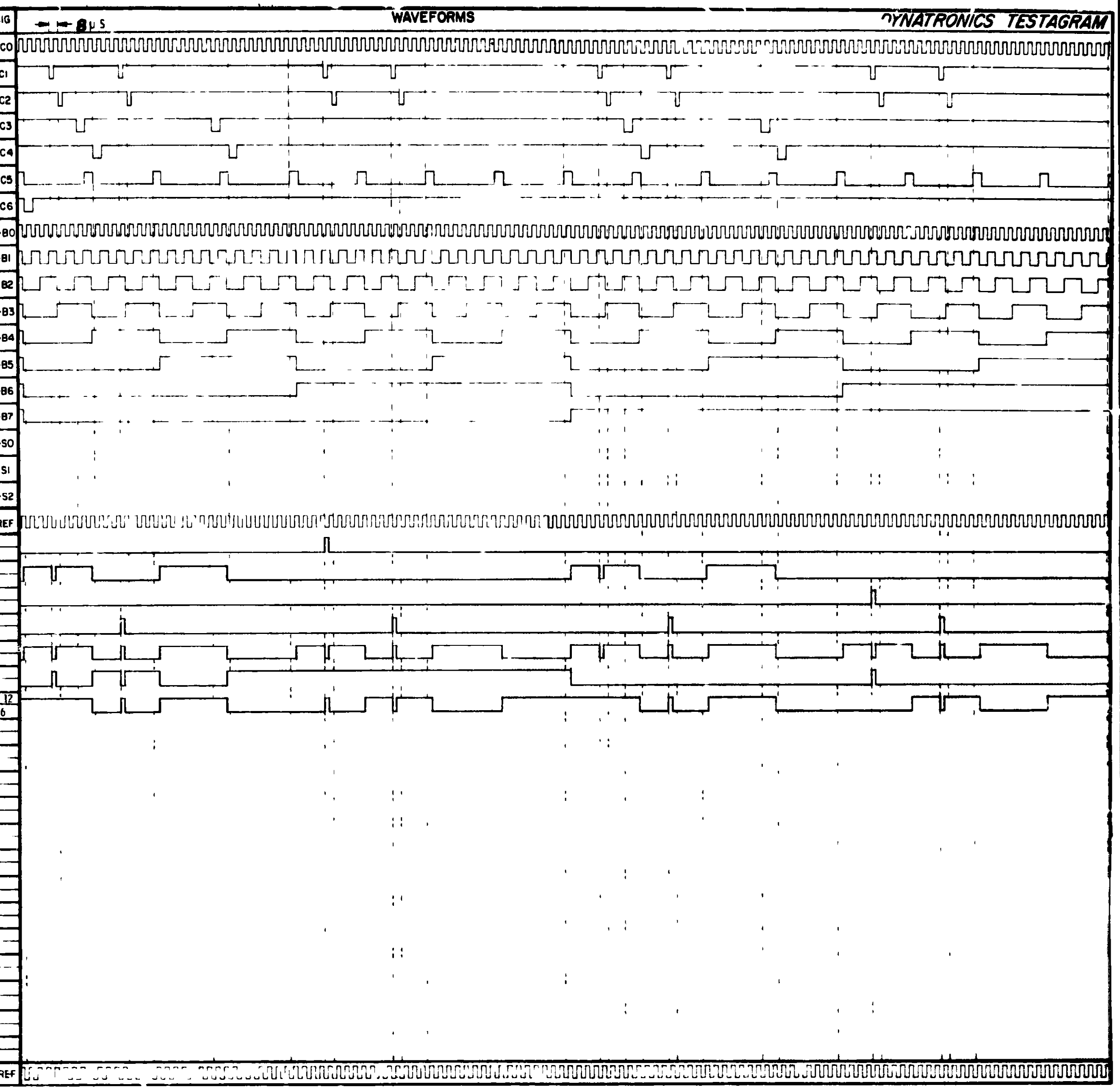
P.C. Logic A52637 Doc. No. 23-1108-22



TEST PARAMETERS			
+Vcc	4.75	SIG V	↑VCC, GRD
±V	——	LOAD REF V	GRD +5V
+V	——	CLK	2μ sec
-V	——	BIT CLK	+OSC

ROW ASSIGNMENT	
10	-C1
1	+B4
2	+B6
3	+B7
4	——
5	GRD
6	+C1
7	—
8	—
9	—

INPUT PINS	COL	SIG
	63	+CO
45 41*	64	C1
	65	-C2
	66	-C3
	67	C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
48 43	74	+B4
	75	+B5
46	76	+B6
40	77	+B7
	78	+S0
	79	+S1
	80	+S2



OUTPUT PINS (TEST POINTS)	SWITCH SETTING												
27	A	1	2	3									
	B	11	2	#									
26	A	1	2	3	4	5	6	7					
	B	2	4	6	1	11	10	5					
15	A	1	2	3									
	B	3	5	#									
(11)	A	1	2	3									
	B	3	5	10									
(25)	A	1	2	3	4	5	6	7	8	9			
	B	2	4	6	1	3	5	11	10	9			
(30)	A	1	2	3	4	5	6	7	8	9	10		
	B	4	6	1	3	5	11	10	5	3	5		
(14)	A	1	2	3	4	5	6	7	8	9	10	11	12
	B	1	3	5	11	10	11	2	8	10	1	7	6

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION
4. ENCIRCLES OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

7-6-71 JN

TEST LEGEND AS APPLICABLE

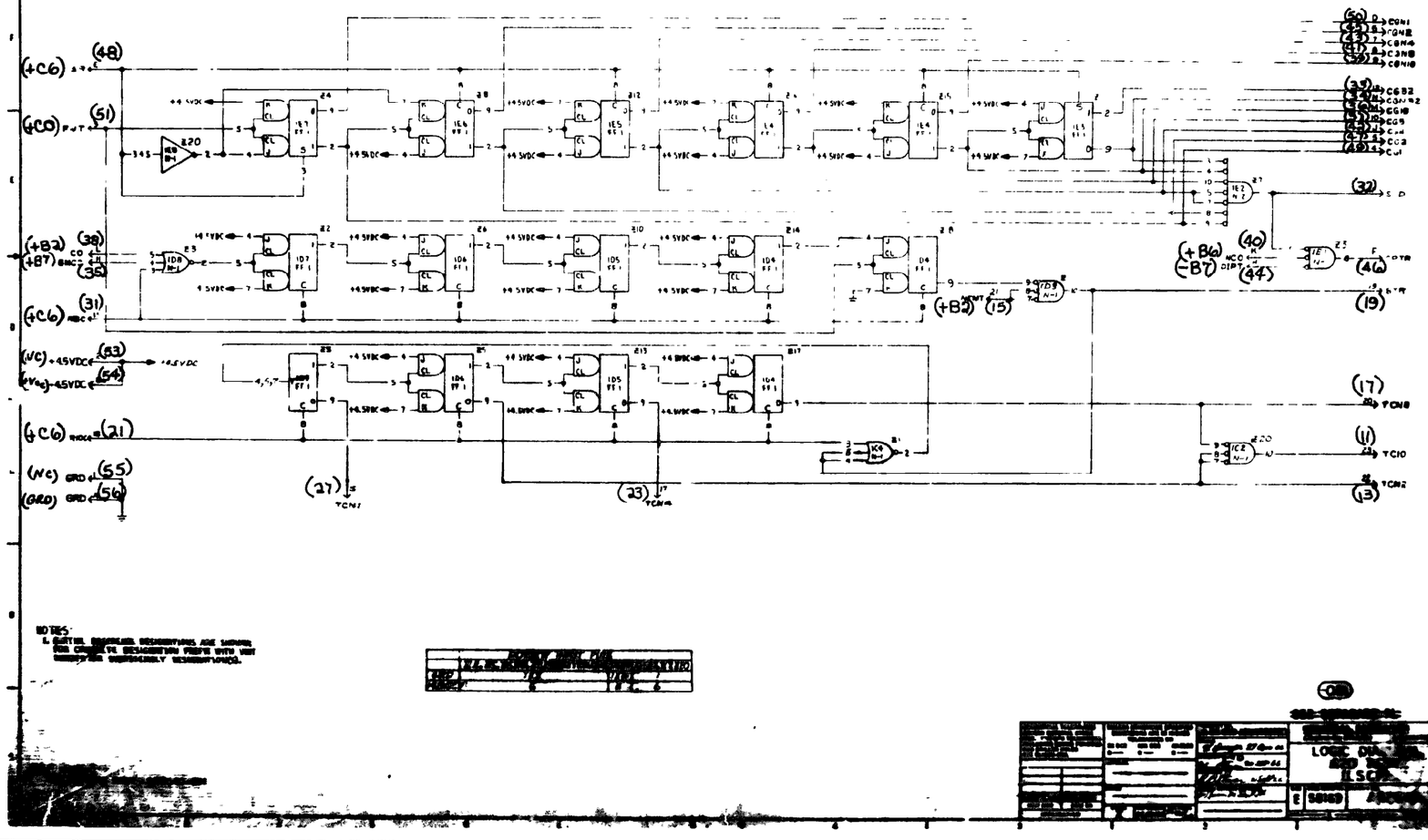
1 ICT —— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

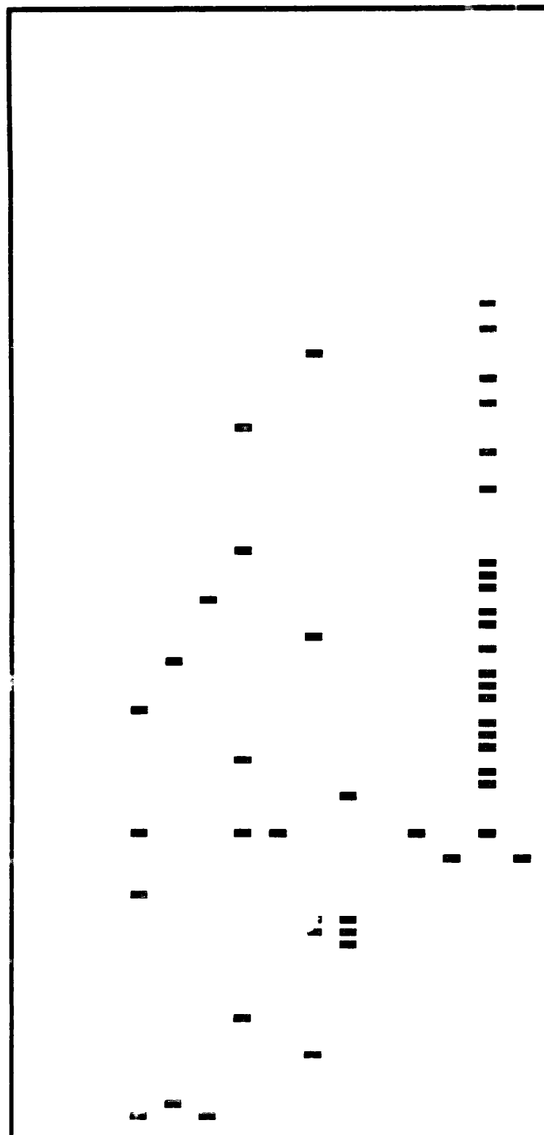
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e , ARE SWITCHING DURING TEST

5 ⋙ INDICATES UNTESTED INPUT/OUTPUT LINES



P.C. Assembly A52646-001

P.C. Logic A52645



A52646-001 DOC. NO. 23-2101-11

GOVT APPD. JW DATE 7-6-71

TEST PARAMETERS			
V_{cc}	+4.75	SIG V	@ 2.5 @ 2.5
ΔV	—	LOAD REF V	@ 2.0
+V	—	CLK	1 μs
-V	—	BIT CLK	+OSC

ROW ASSIGNMENT	
10	—
1	—
2	—
3	*C0
4	*B7
5	—
6	*C6
7	*B7
8	*B6
9	-B7

INPUT PINS	COL.	SIG
51	63	+C0
	64	C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
48, 31, 21	69	-C6
	70	+B0
	71	+B1
15 38	72	+B2
	73	+B3
	74	+B4
	75	+B5
40	76	+B6
44, 35	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POIN S)	SWITCH SETTING	+CO REF
50, 49	A 1 2 3 4 / B 11 4 8 1	
65, 47	A 1 2 3 4 / B 3 11 8 5	
43, 42*	A 1 2 3 4 / B 3 8 2 7	
41, 37	A 1 2 3 4 / B 3 2 1 11	
39, 36*	A 1 2 3 4 / B 3 1 10 8	
33, 34	A 1 2 3 4 / B 3 10 6 2	
46	A 1 2 3 4 / B 5 9 10 1	
(32)	A 1 2 3 / B 6 10 4	
19	A 1 2 3 4 / B 2 3 9 6	
27	A 1 2 3 4 / B 2 3 9 3	
13	A 1 2 3 4 / B 3 2 1 11	
23	A 1 2 3 4 / B 2 11 9 7	
17	A 1 2 3 4 / B 3 11 7 3	
(11)	A 1 2 3 4 / B 10 9 8 7	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	

WAVEFORMS — DYNATRONICS TESTAGRAM

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS 'B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

TEST LEGEND AS APPLICABLE

1 ICT ——— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

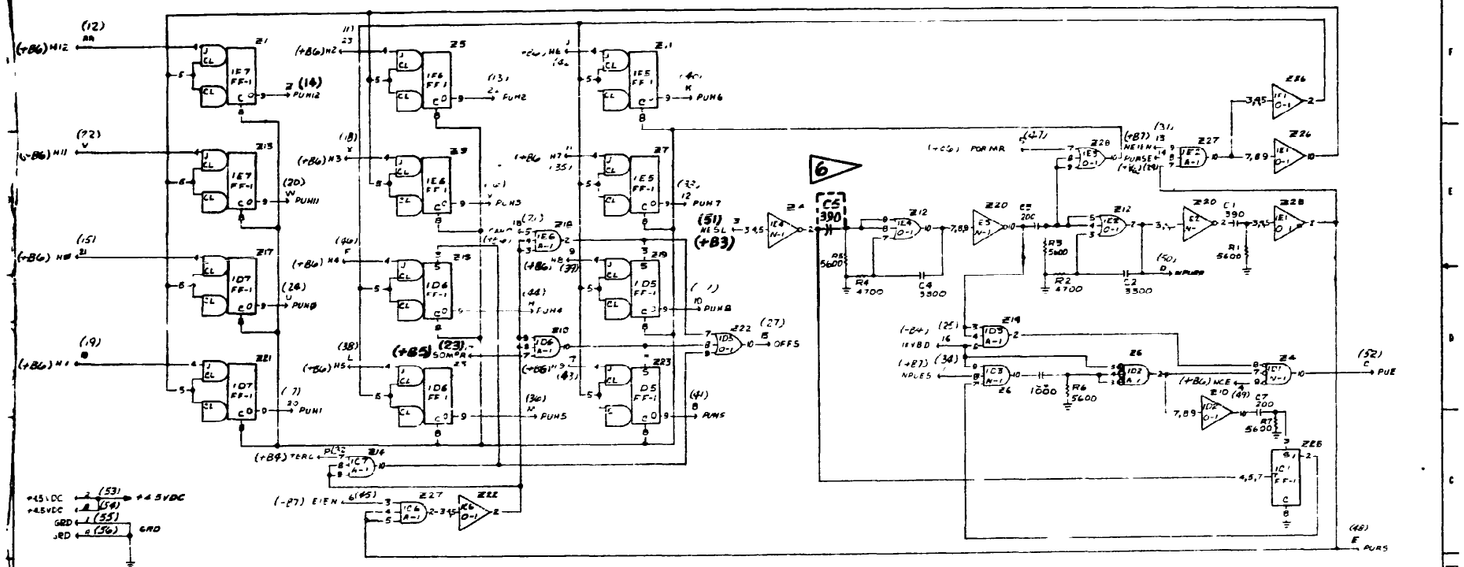
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST

5 ⩫ INDICATES UNTESTED INPUT/OUTPUT LINES

6 INSTALL JUMPER ACROSS C5 BEFORE TESTING CARD.



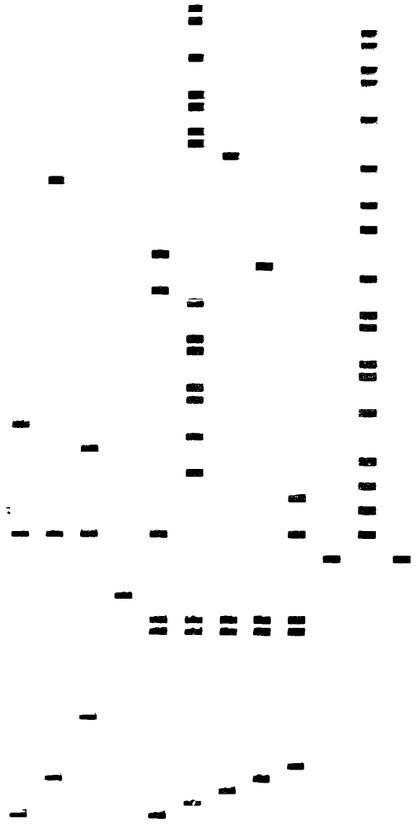
NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATIONS WITH UNIT NUMBER CONSULT ASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR RATINGS ARE 1/4 W
   ALL RESISTOR TOLERANCES ARE ±5%
   ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS.

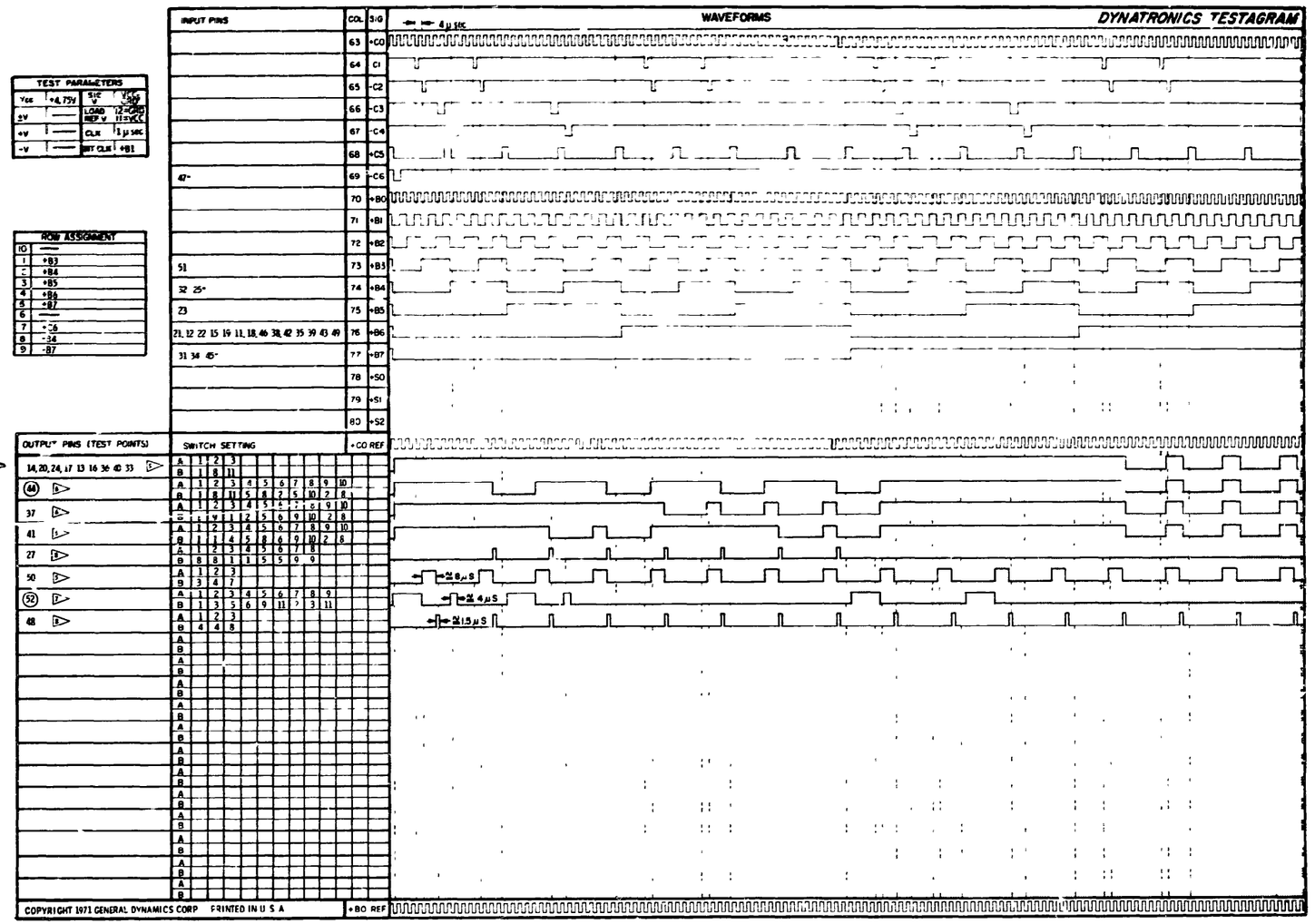
REF DWG

MECH ASSY ——— A52657-001

POWER INPUT PINS			
Z7,24,26,Z15,E 2,2 4,E16, F16,Z13,Z22,,E25 THRU E28		Z15 Z19,Z23	Z1,Z5,Z6,Z7,Z9 Z11,Z13,Z17,Z21
GND		1	4,7	1,3,7
+5VDC		6	6	6

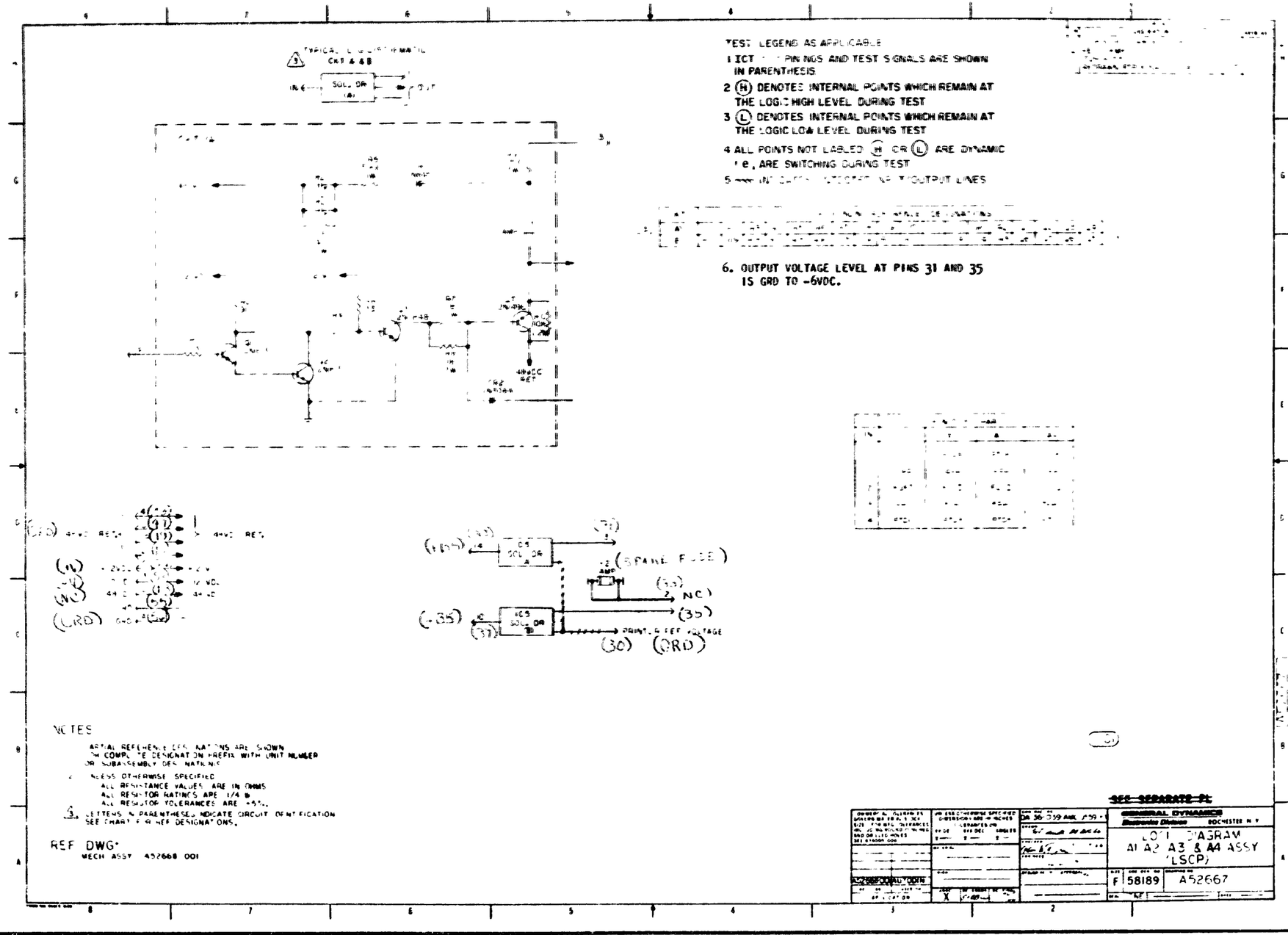


A52657-001 DOC. NO. 23-2102-11



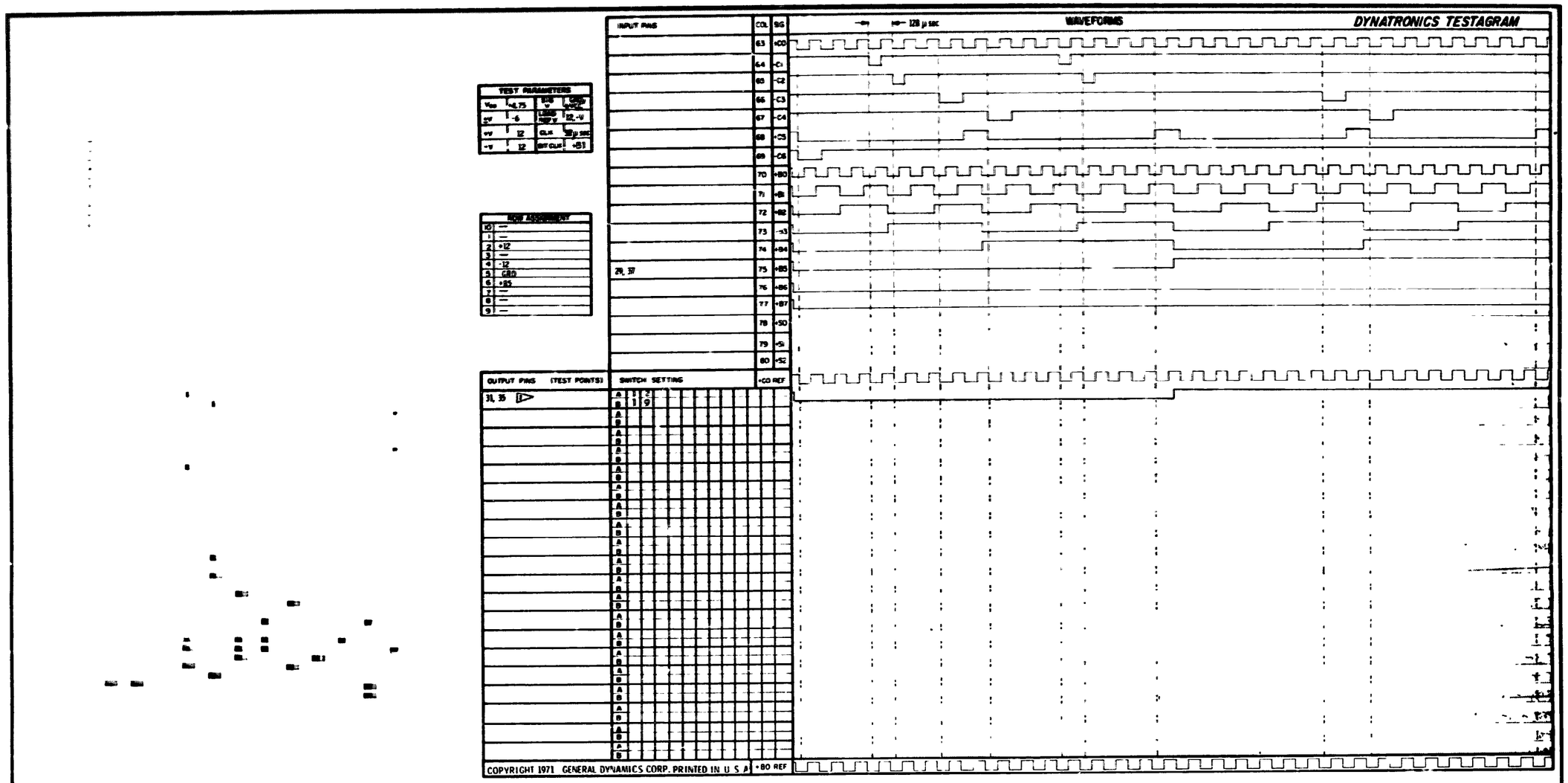
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. INSTALL JUMPER ACROSS C5 BEFORE TESTING.
5. EDGE A2 MAY BE ± 1 "B" SWITCH POSITION FROM THE ONE SHOWN FOR A "GO" INDICATION.
6. EDGES A2, 4, 6, 8 and 10 MAY BE ± 1 "B" POSITION.
7. EDGES A4 and A8 MAY BE ± 1 "B" POSITION.
8. ALL EDGES MAY BE ± 1 "B" POSITION.



P.C. Assembly A52638-001

P.C. Logic A52567

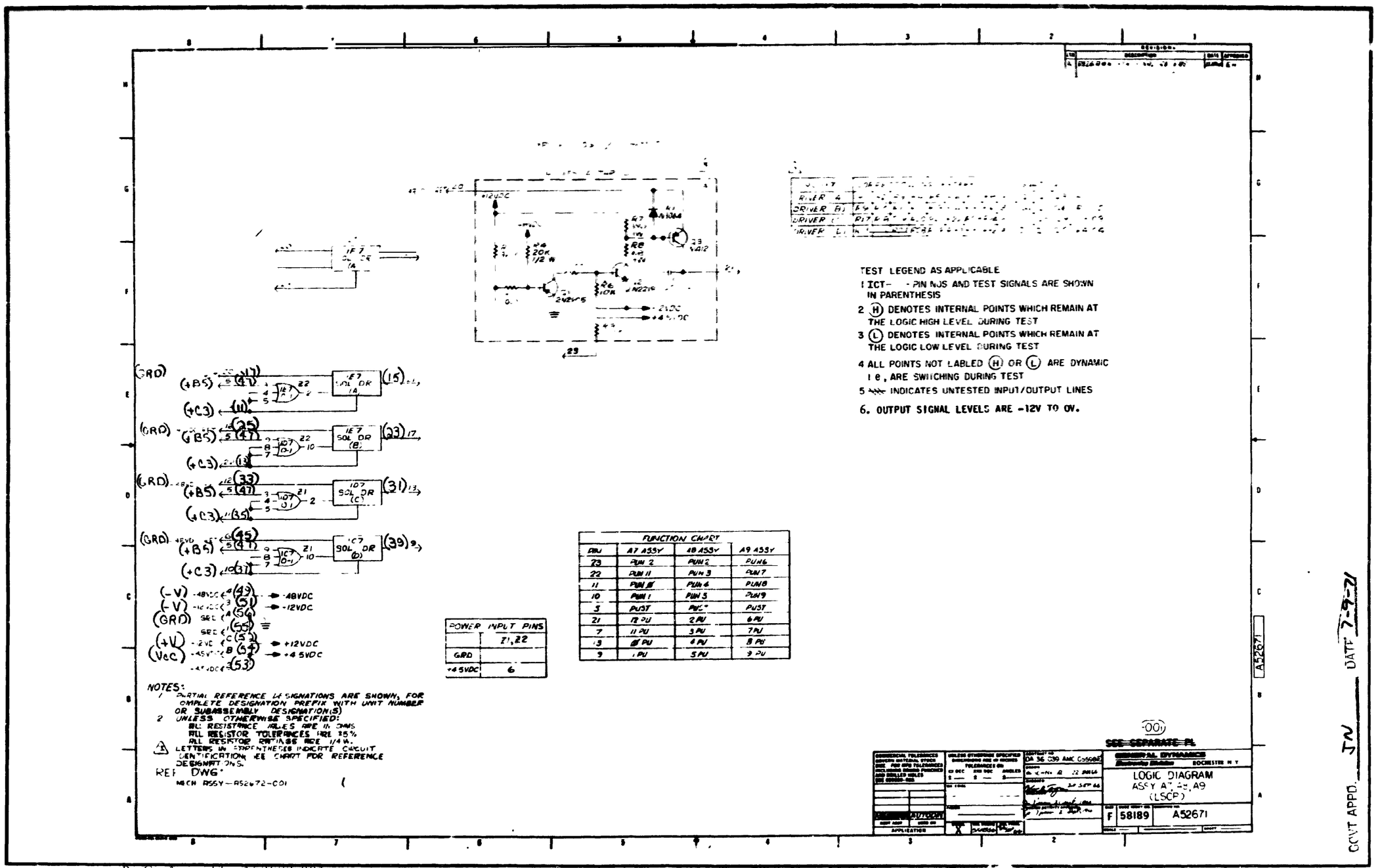


NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. OUTPUT VOLTAGE LEVEL AT PINS 31 AND 35 IS GRD TO -6 VDC.

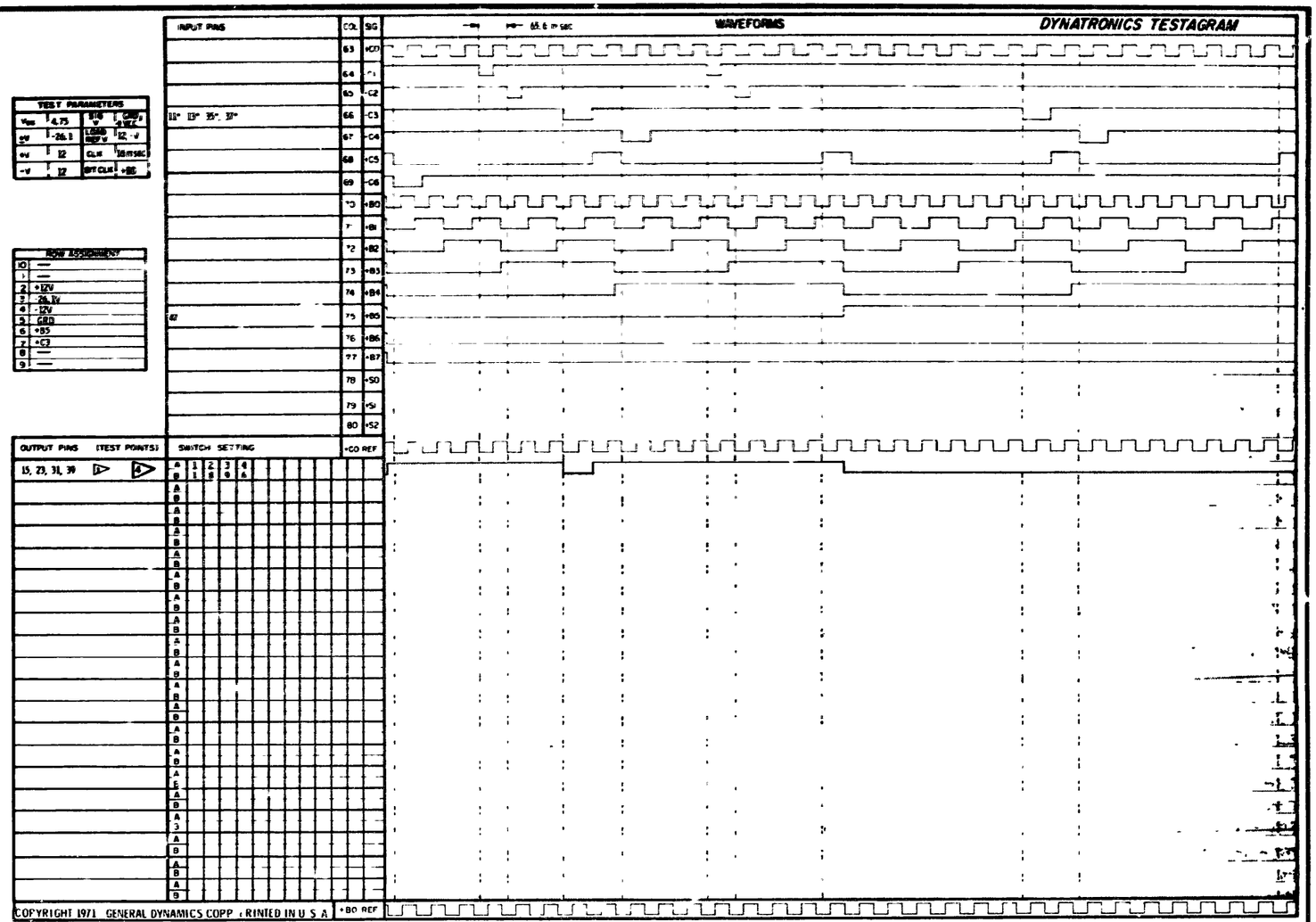
A52668-001 DOC. NO. 23-2103-11

GOVT APPD. JN DATE 7-9-71



P. C. Assembly A52672-001

P. C. Logic A52671

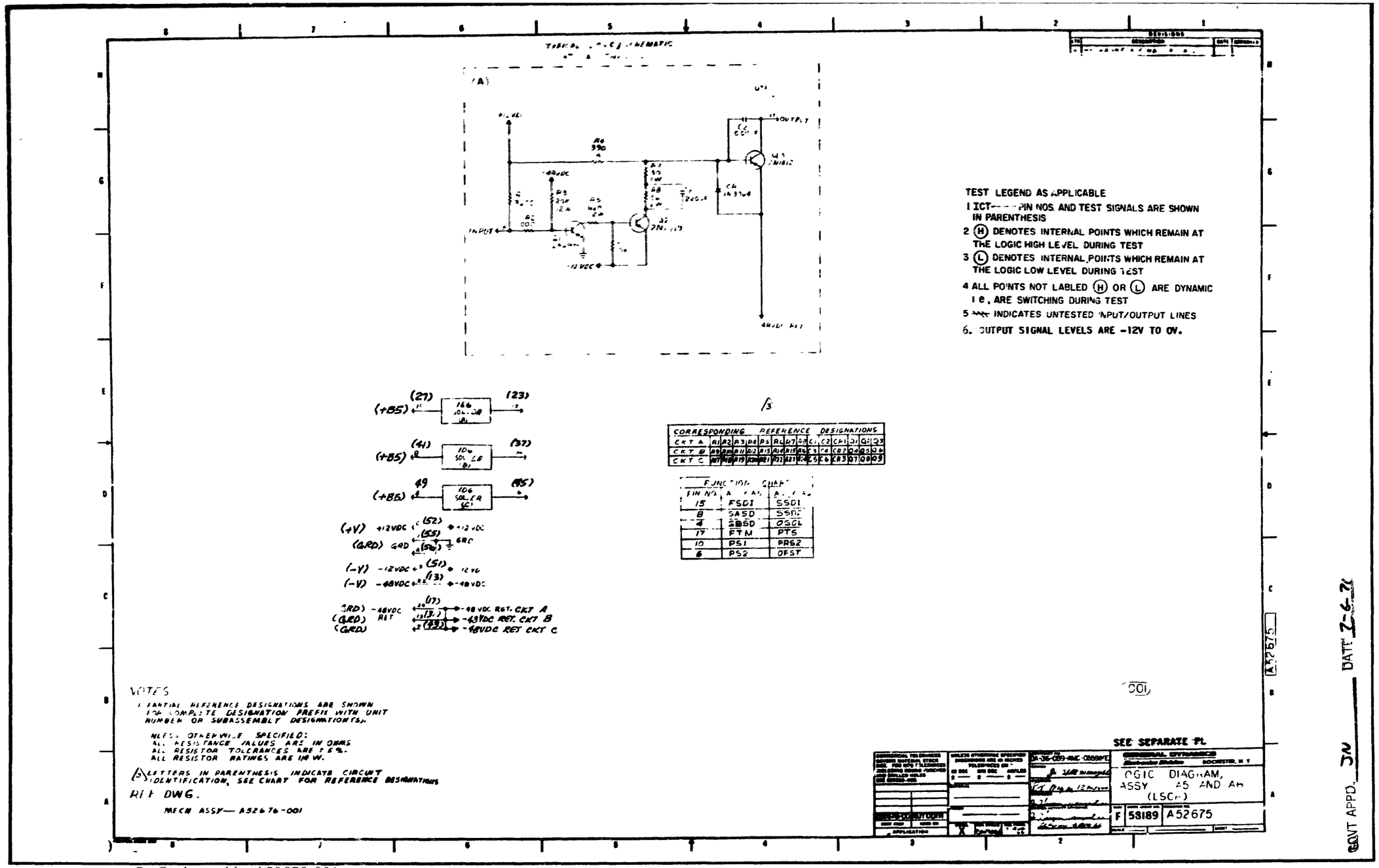


NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. OUTPUT SIGNAL LEVELS ARE -12V TO 0V.
4. GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.

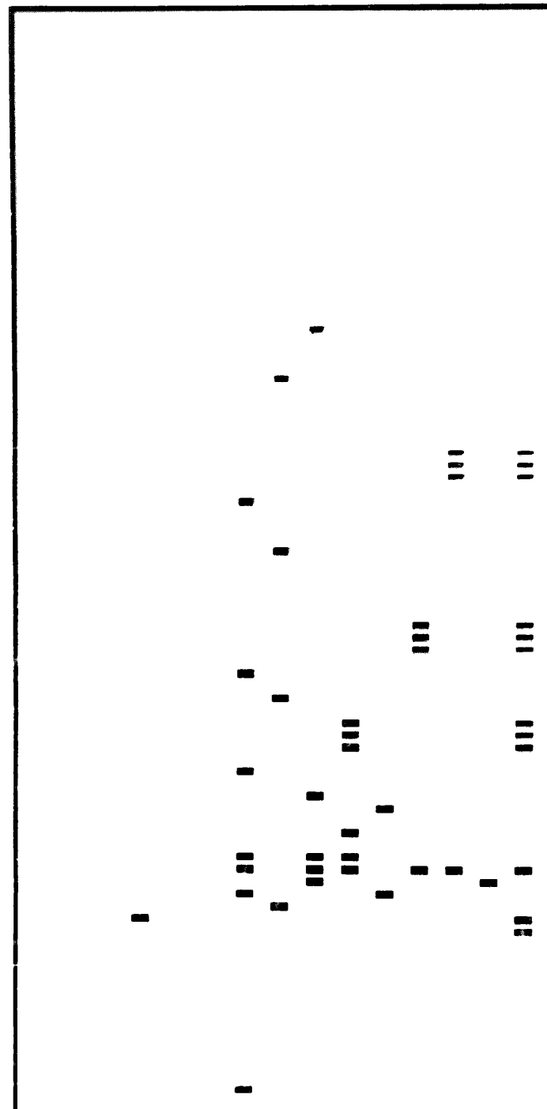
A52672-001 DOC. NO. 23-2104-11

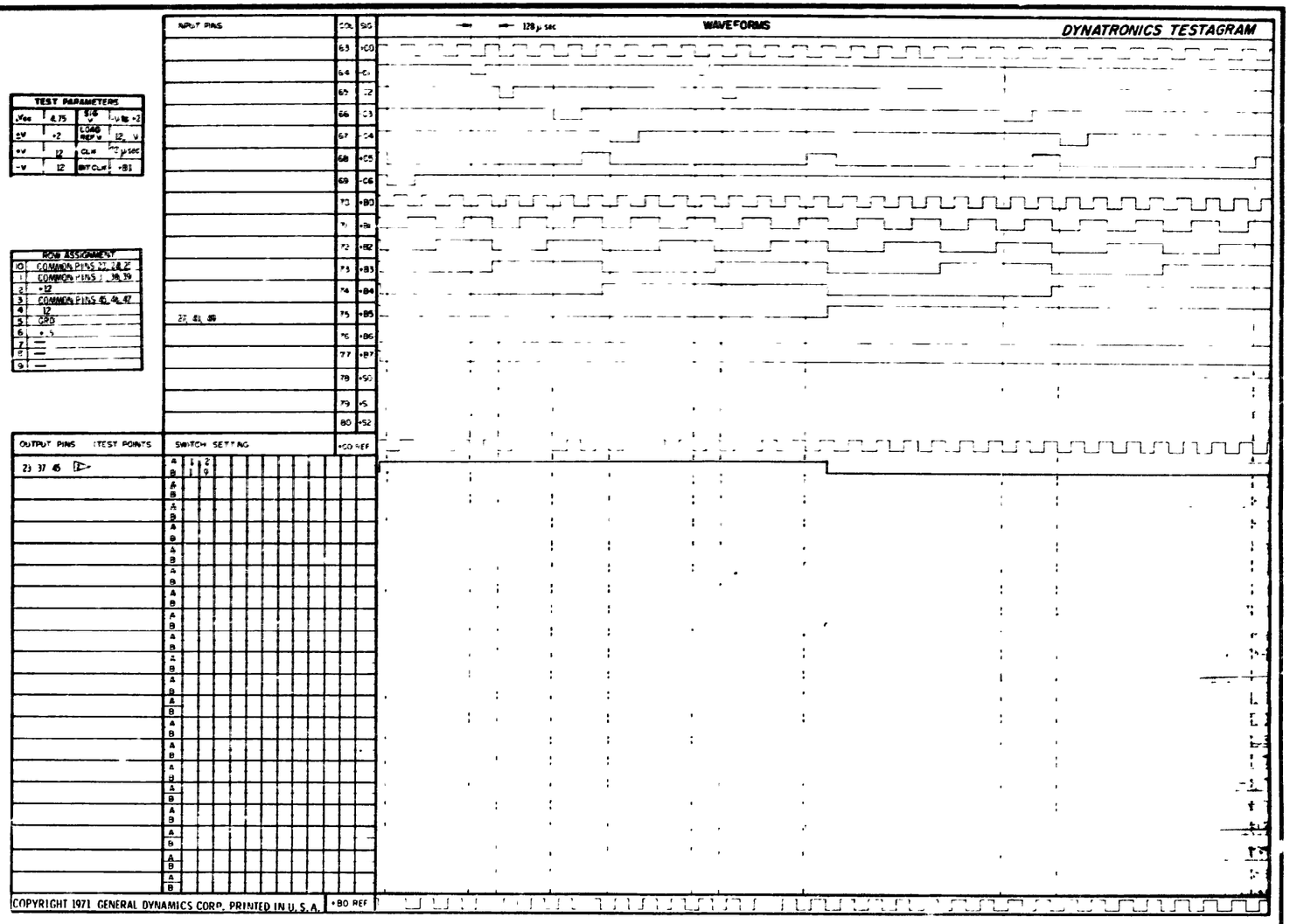
...VT APPD. JN DATE 2-9-71



P. C. Assembly A52676-001

 P. C. Logic A52675





NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. OUTPUT SIGNAL LEVELS -12V TO 0V.

A52676-001 DOC. NO. 23-2105-11

GOVT APPD. JN DATE 2-6-71

TEST LEGEND AS APPLICABLE

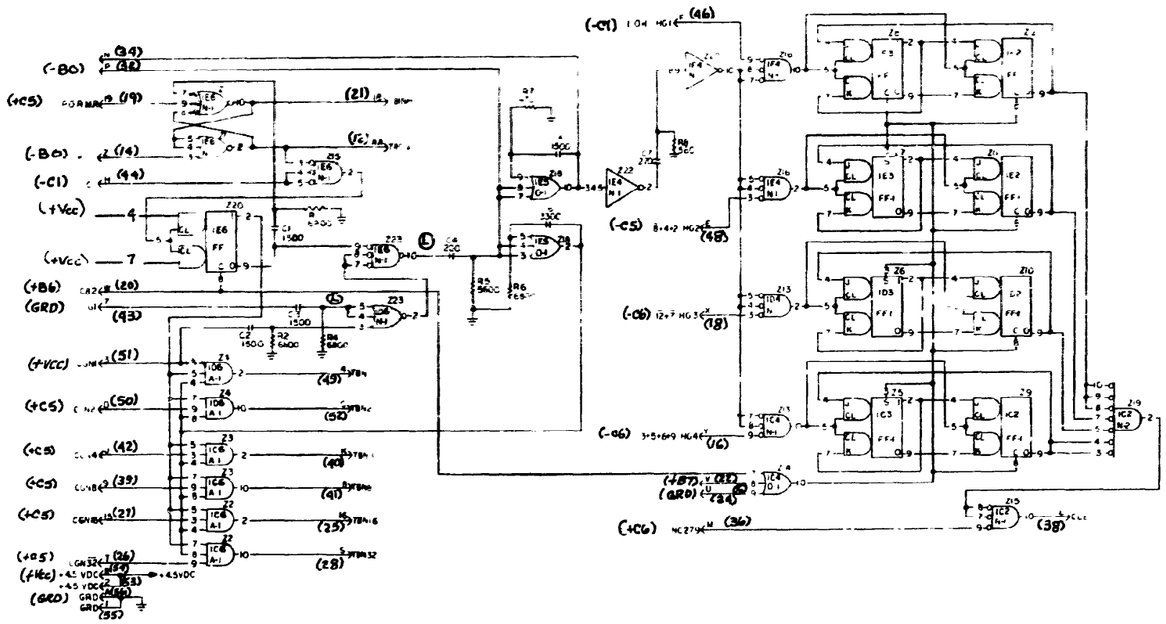
1 ICT — PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e , ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES



NOTES

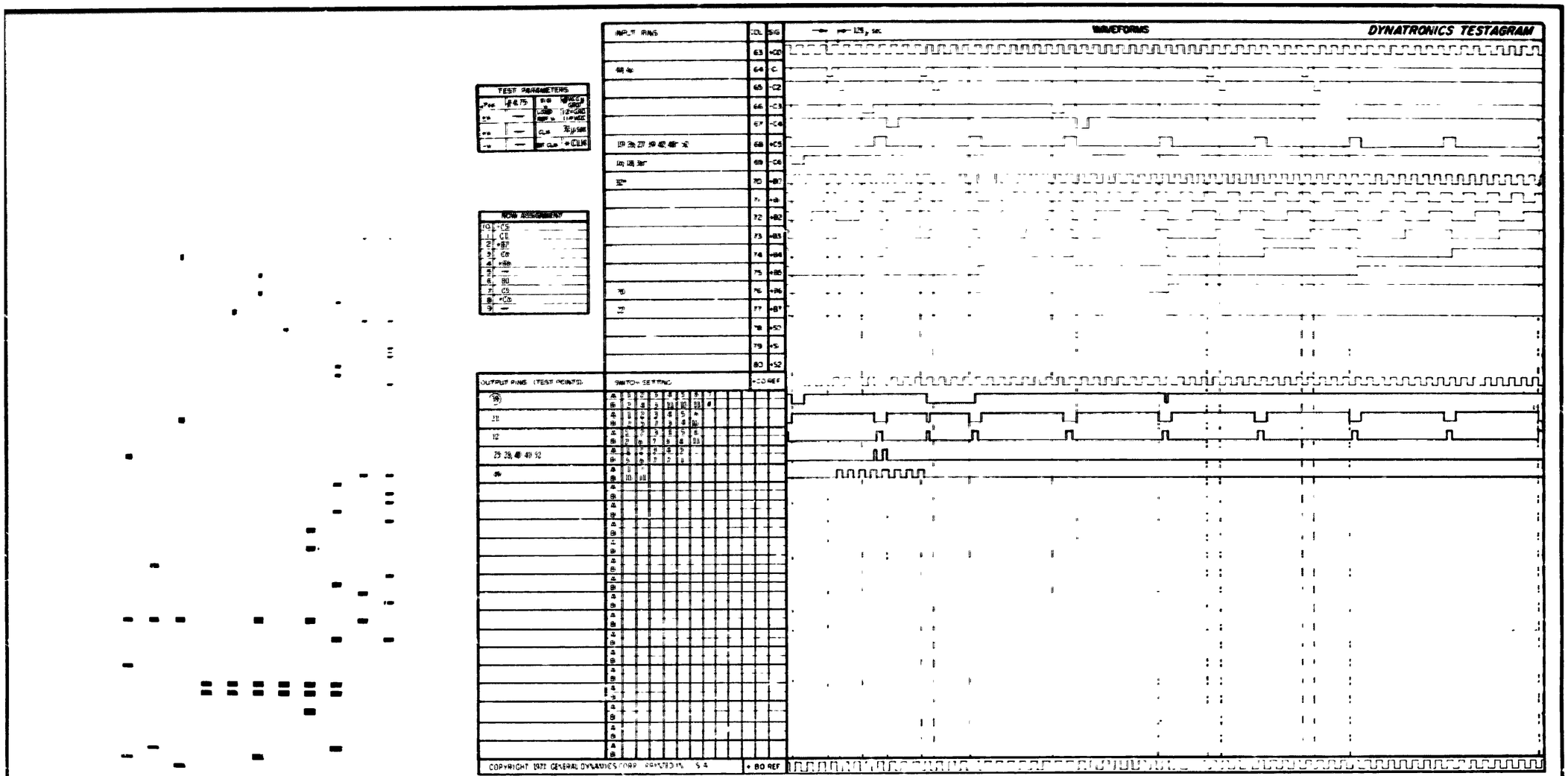
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION USE
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR RATINGS ARE ¼W
   ALL RESISTOR TOLERANCES ARE ±5%
   ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS

REF DWG
MFR ASSY - A52710-001

7-6-71 JN.

P.C. Assembly A52710-001

P.C, Logic A52709



A52710-001 DOC. NO. 23-1109-12

7-6-71 JN

NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" : VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

TEST LEGEND AS APPLICABLE

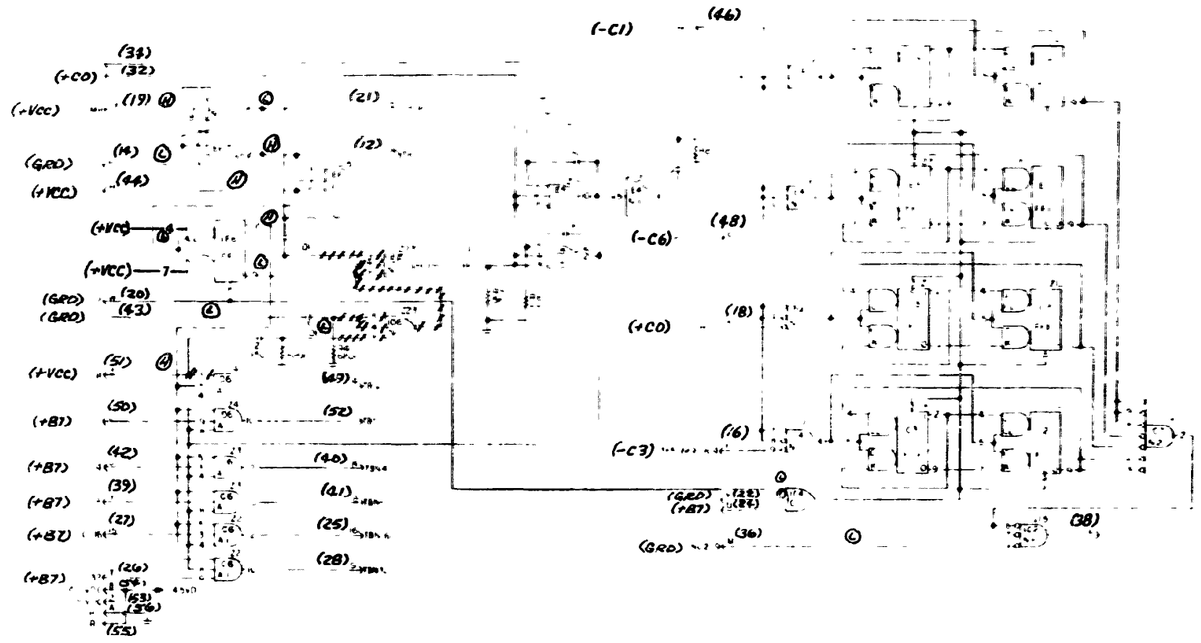
1 ICT- —— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES



NOTES:

1. ALL RESISTANCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION ON REF. WITH UNIT NUMBER (XX-XXXXXX-XXX) SUBASSEMBLY DESIGNATION IS:
   UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR RATINGS ARE 1/4W
   ALL RESISTOR TOLERANCES ARE ±5%
   ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS
2. W1

POWER INPUT PINS					
	37 THRU 24, 35 THRU 28, 26, 25 THRU 21				
GRD	54, 70, 71, 72, 73, 74	77	75	76	56
+5VDC	67	68	69	66	57

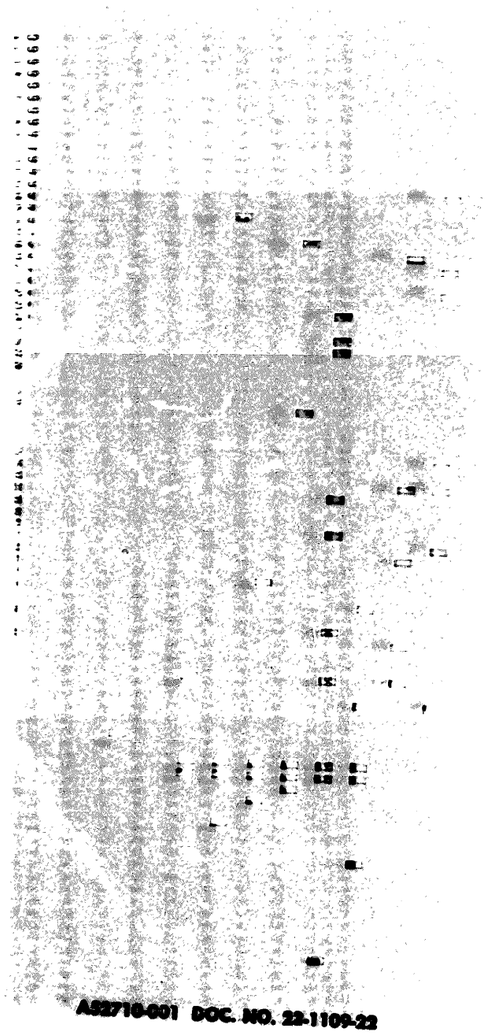
SEE SEPARATE PL

LOGIC DIAGRAM
ASSY
SCP

E 58189 A52709

7-6-71 JN

P.C. Assembly A52710-001
P.P. Logic A52709



TEST PARAMETERS

ROW ASSIGNMENT

10	C8
1	+B7
2	+C8
3	C8
4	C1
5	—
6	—
7	—
8	—
9	—

INPUT PINS | COL | S-G

OUTPUT PINS (TEST POINTS) | SWITCH SET NG

WAVEFORMS — DYNATRONICS TESTAGRAM

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NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.

7-6-71 JN

TEST LEGEND AS APPLICABLE

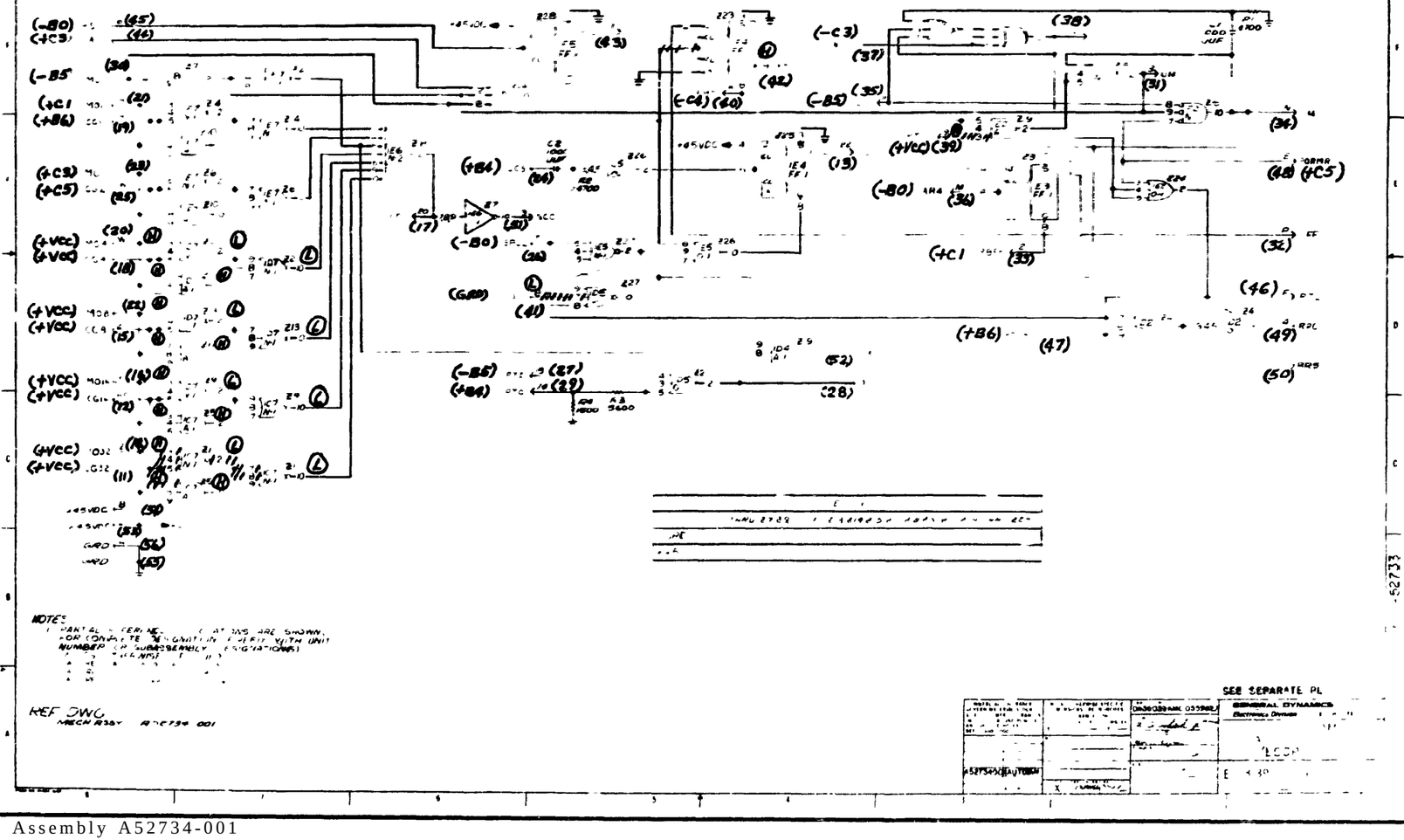
1 ICT—— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES



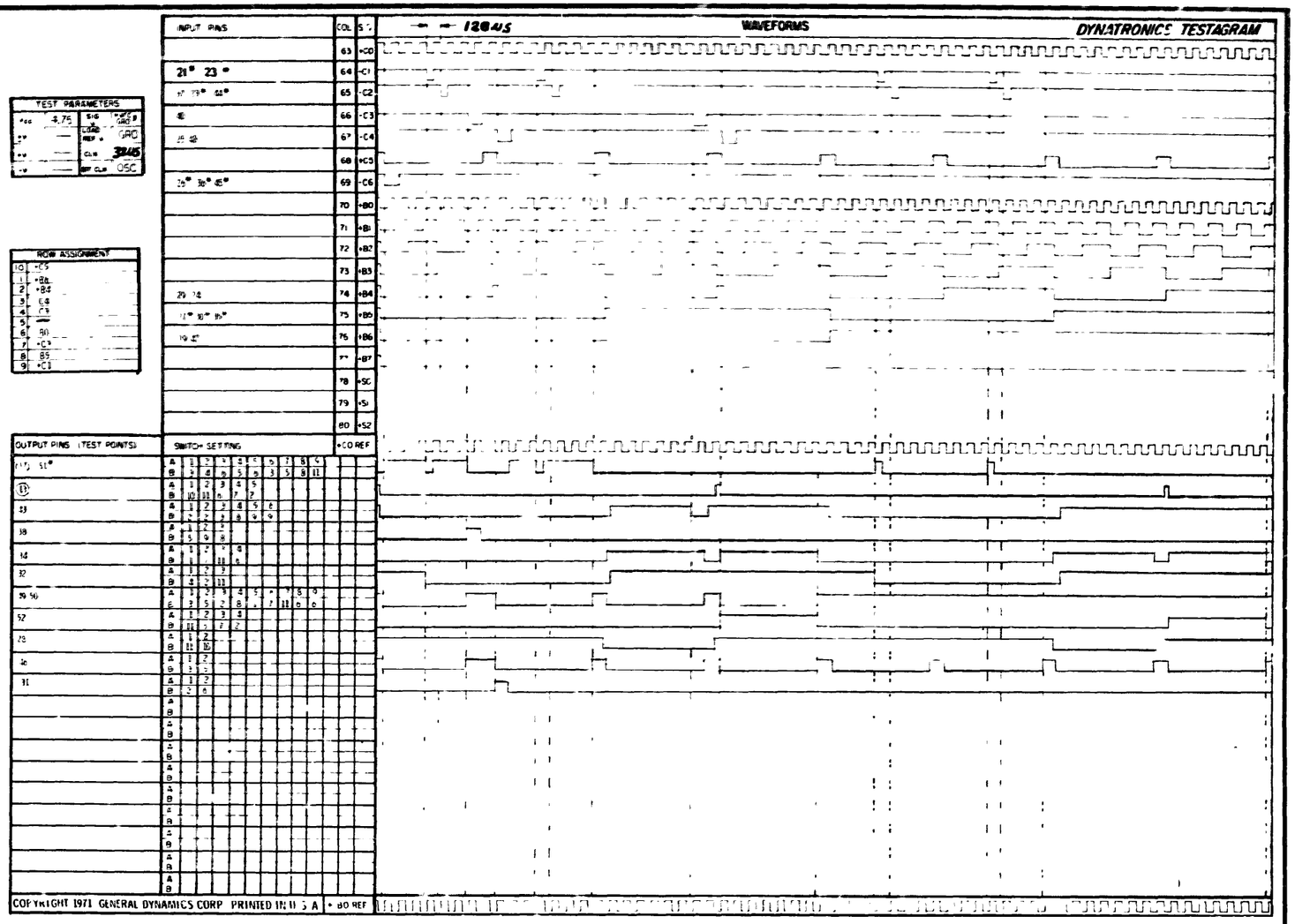
NOTES

REF DWG

SEE SEPARATE PL

-52733

7-C-71 JN

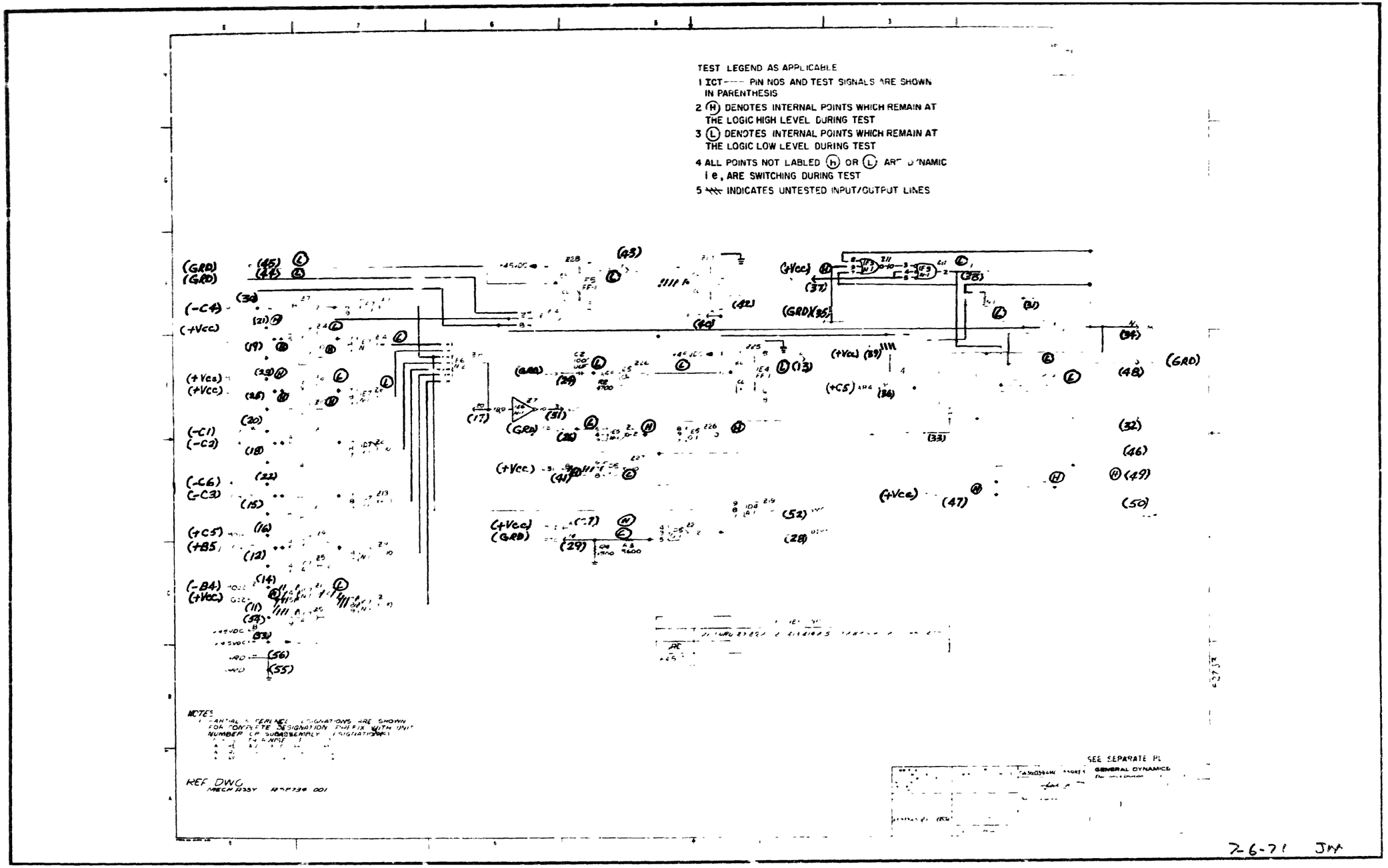


A52734-001 DOC. NO. 23-1110-12

NOTES:

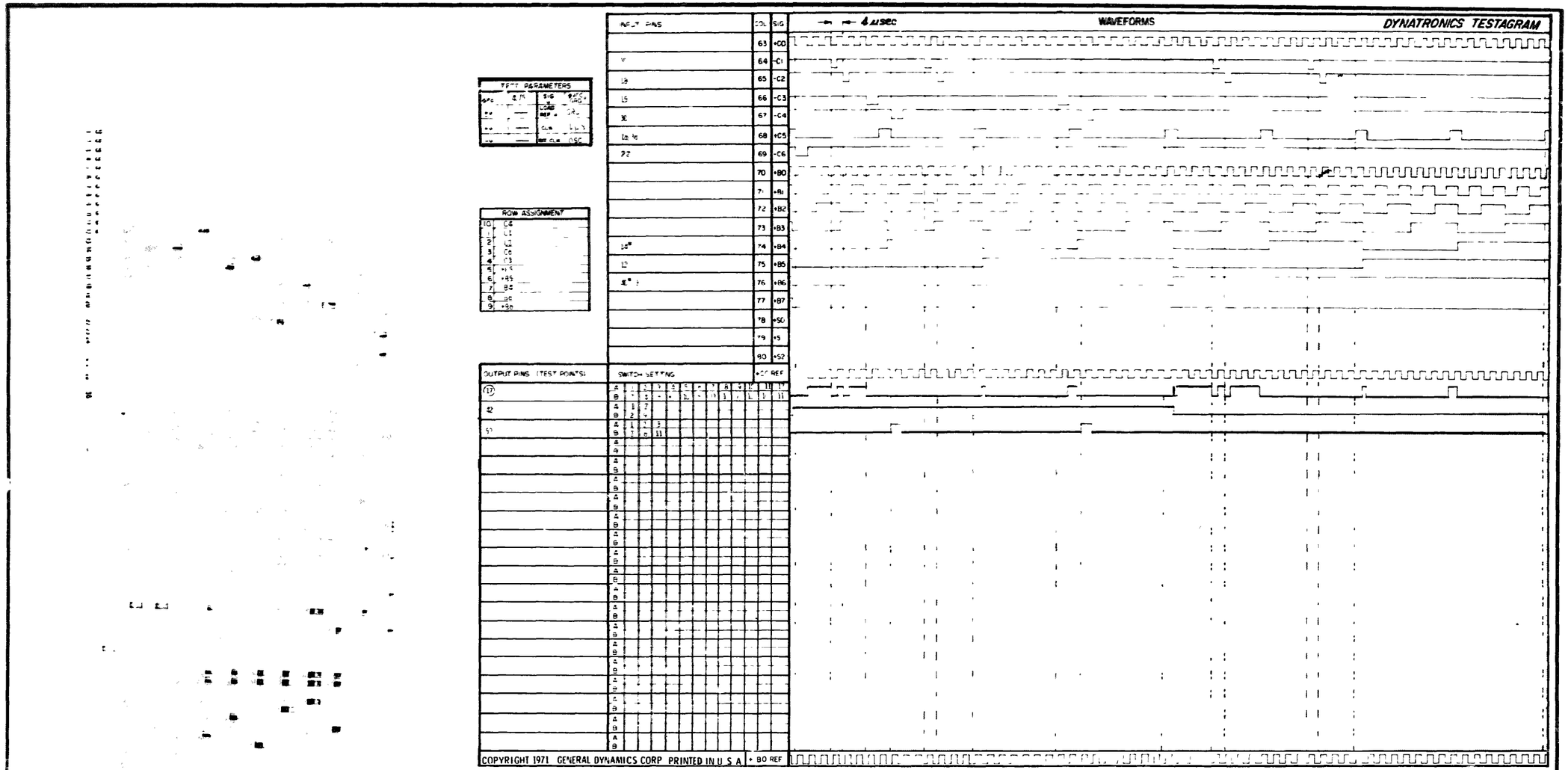
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

7-6-71 JN



P.C. Assembly 52734-001

 P.C. Logic A52733 Doc. No. 23-1110-22

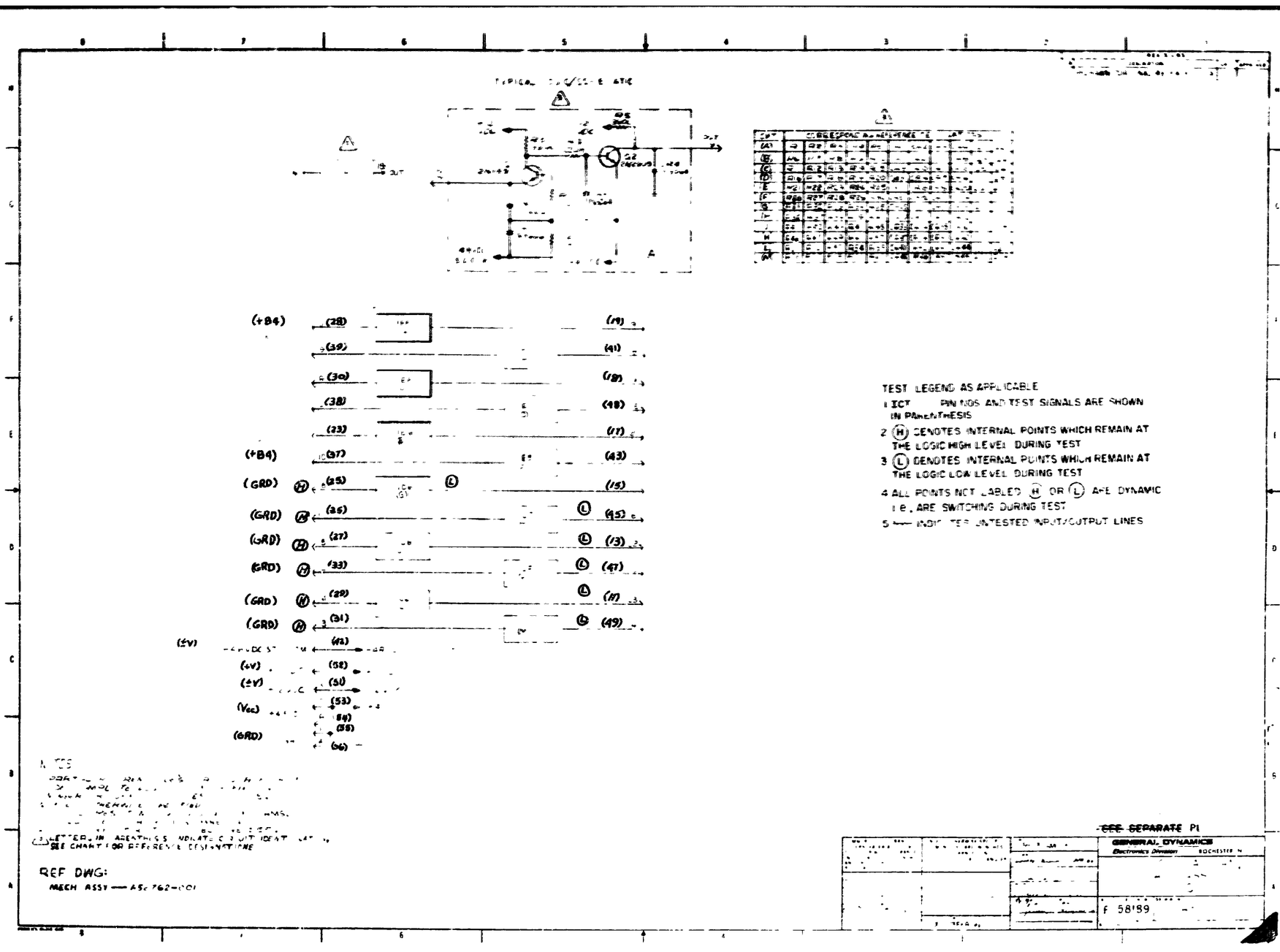


A52734-001 DOC. NO. 23-1110-22

NOTES:

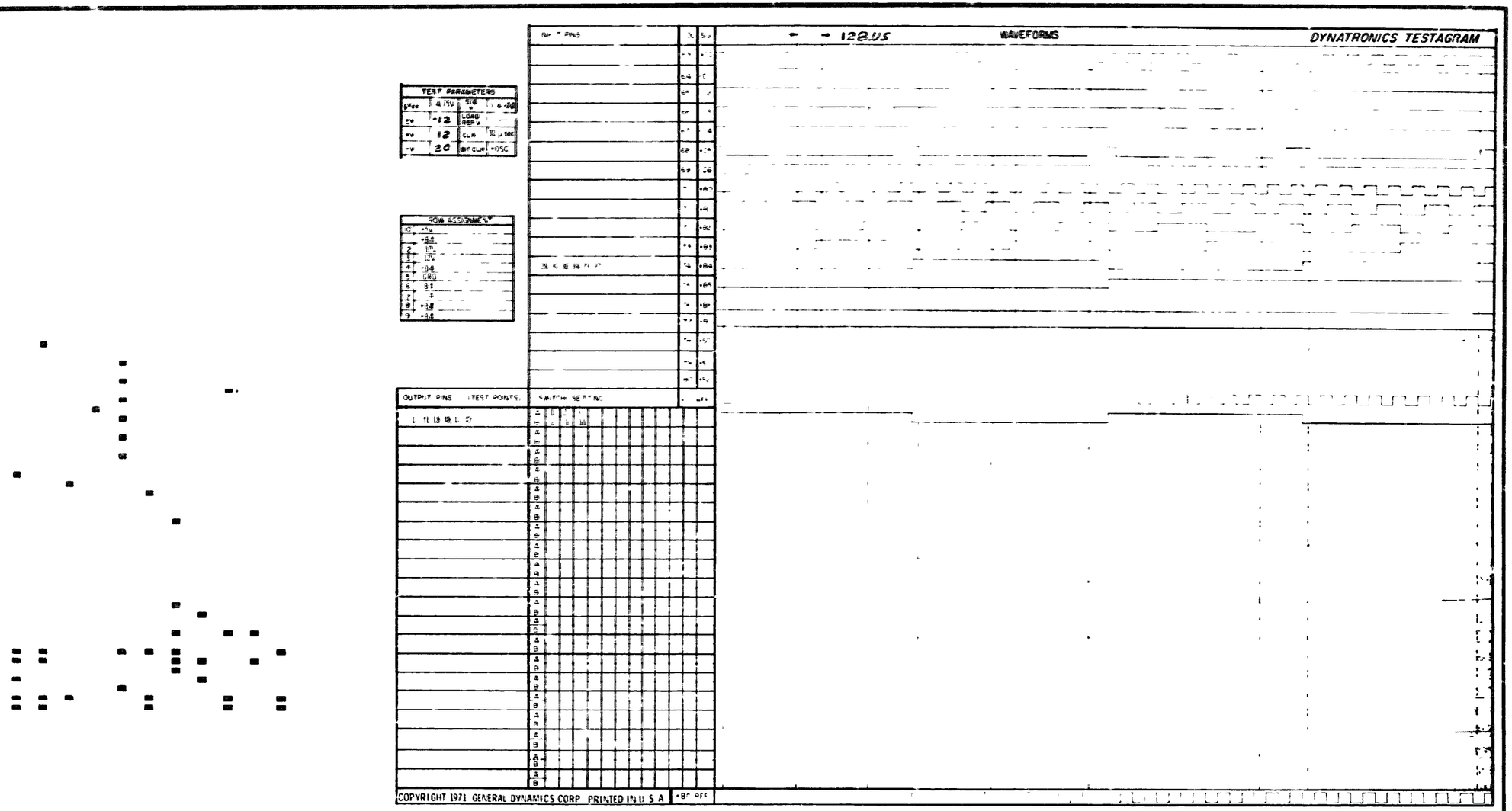
1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

7-6-71 JN



P.C. Assembly A52762-001

P.C. Logical A52761

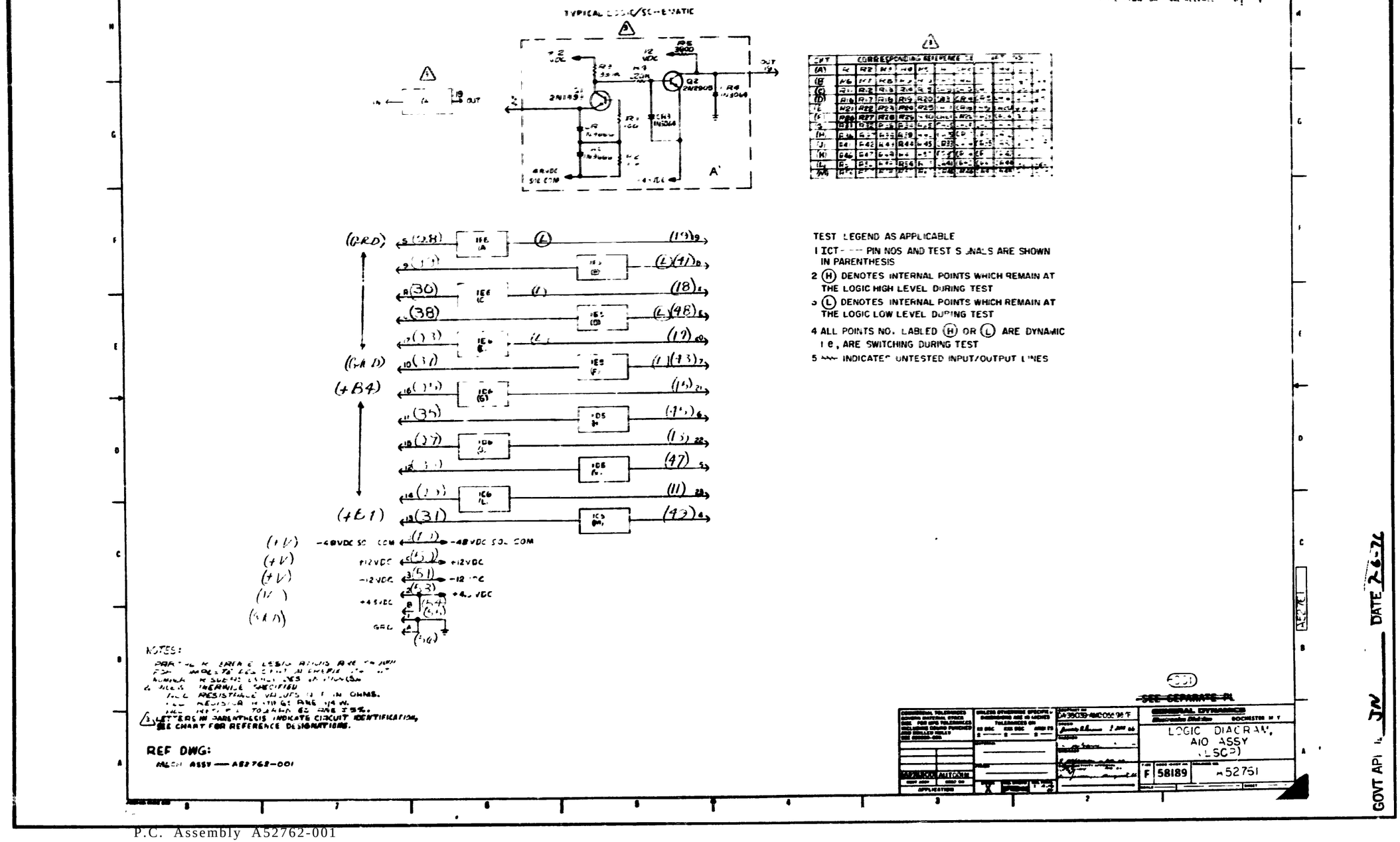


NOTE:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +5.75V.

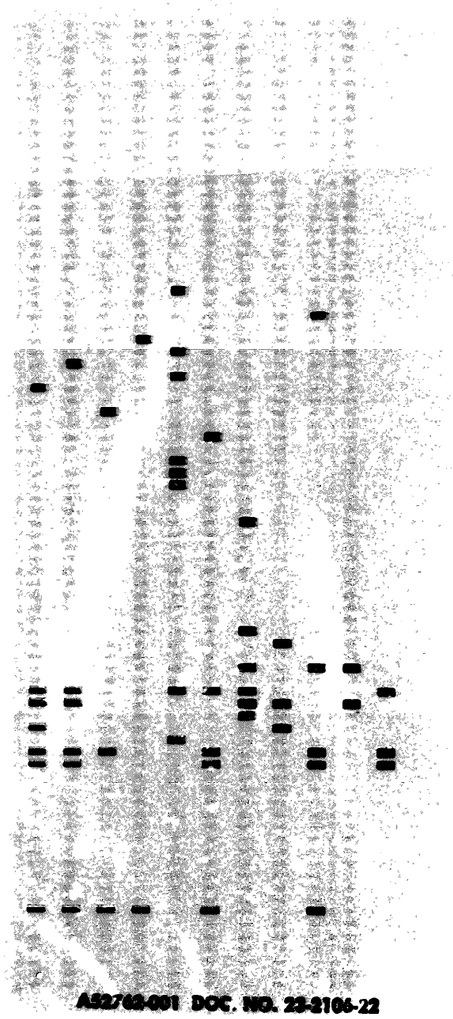
A52762-001 DOC. NO. 23-2105-12

GOVT APPD. JN DATE 7-6-71

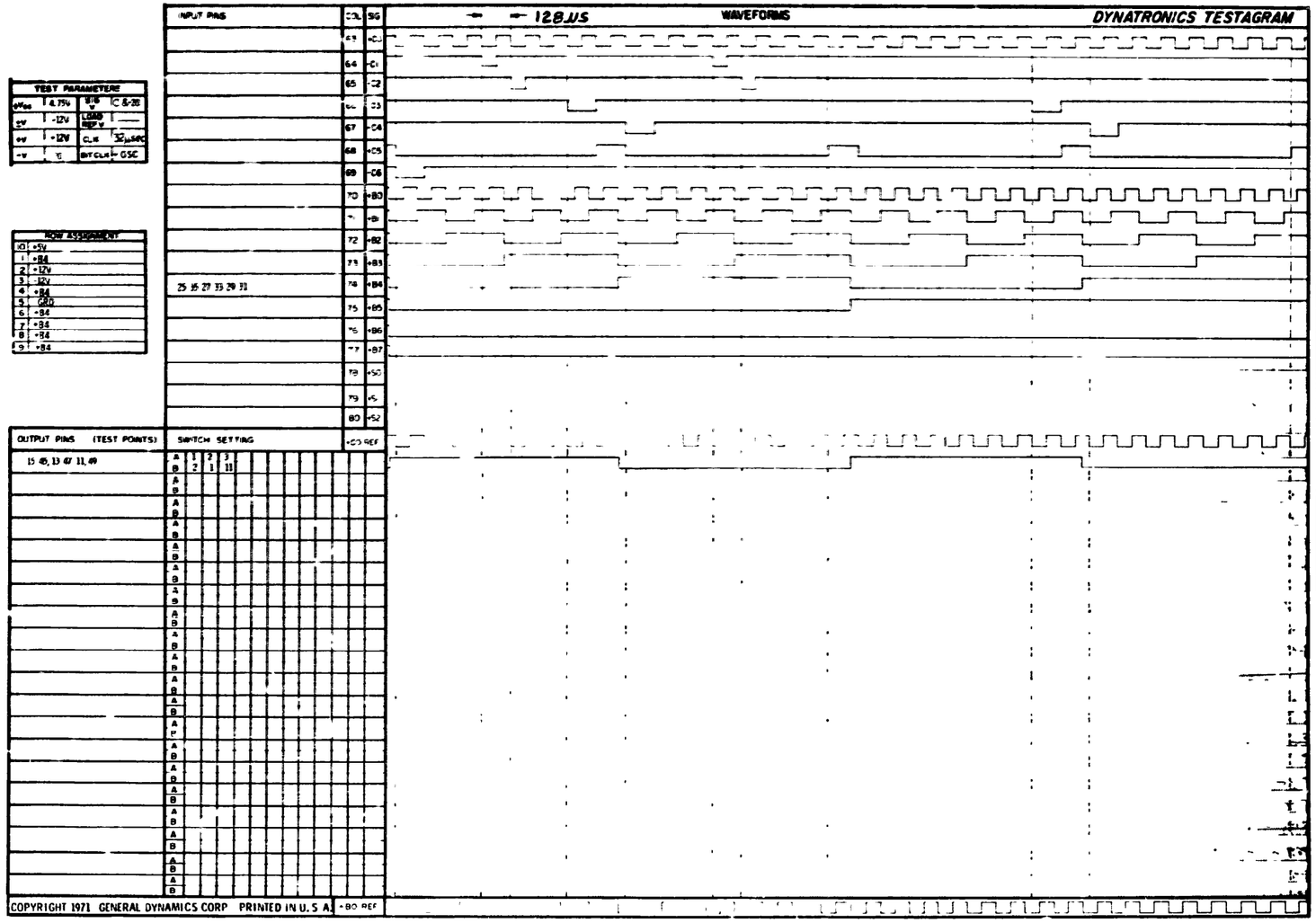


P.C. Assembly A52762-001

P.C. Logic A52761 Doc. No. 23-2106-22



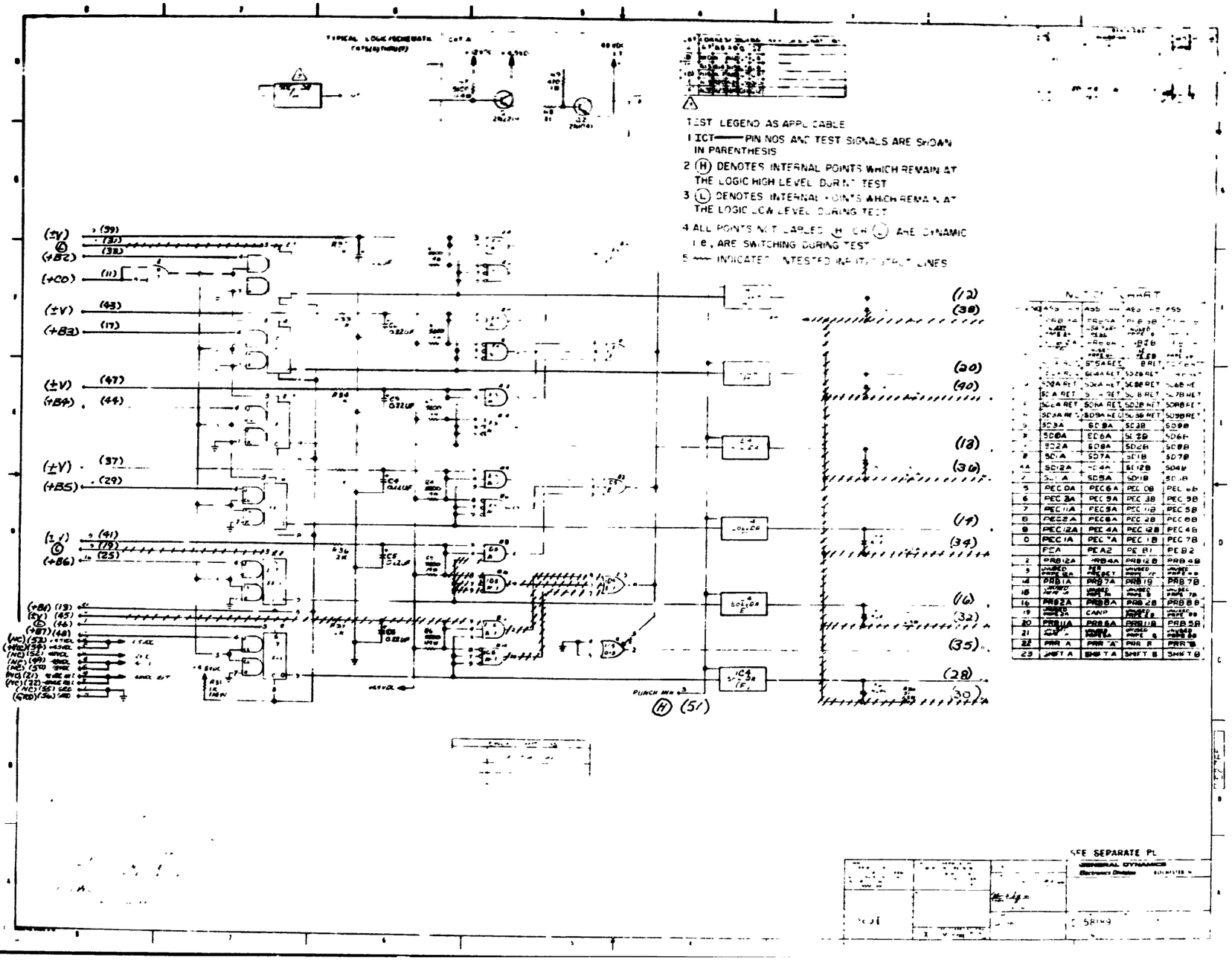
A52762-001 DOC. NO. 23-2106-22



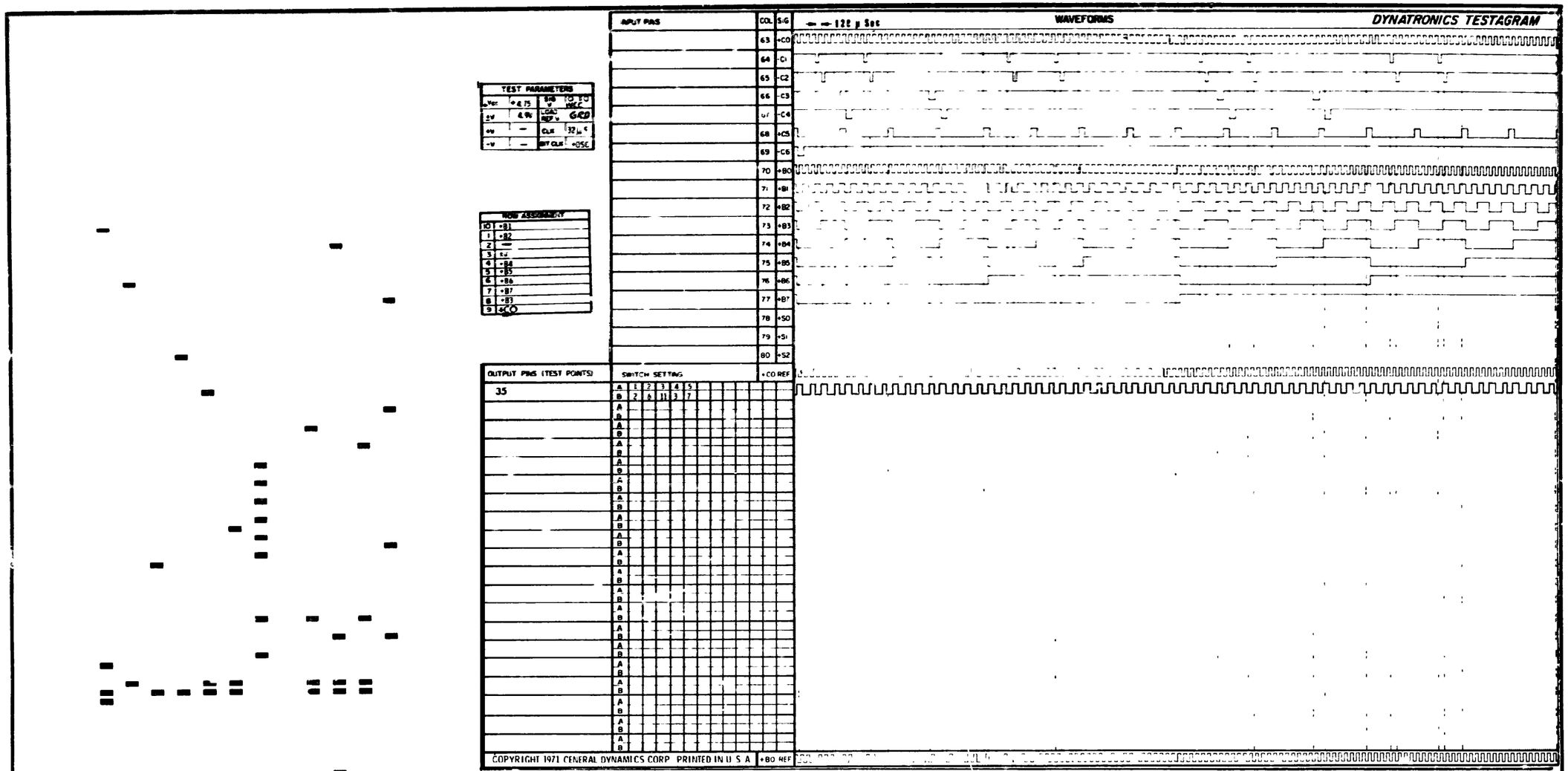
NOTE:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

GOVT APPD. JN DATE 2-6-71



P.C. Assembly A52766-001
P.C. Logic A52765



NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO 4.75V.

A52766-001 DOC. NO. 23-1111-12

JN DATE 7-7-71

TEST LEGEND AS APPLICABLE

1 ICT- PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.e., ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES

FUNCTION CHART

PIN NO	ASSY A3	ASSY A4	ASSY A5	ASSY A6
F	PRB 3A	PRB 9A	PRB 3B	PRB 9B
E	SHIFT PRB 3A	SHIFT PRB 9A	SHIFT PRB 3B	SHIFT PRB 9B
H	PRB 6A	PRB 6A	PRB 6B	PRB 6B
J	SHIFT PRB 6A	SHIFT PRB 6A	SHIFT PRB 6B	SHIFT PRB 6B
N	SC A RET.	SD5A RET.	SC 4B RET.	SD5B RET.
L	SC2A RET.	SD4A RET.	SD2B RET.	SD4B RET.
M	SD8A RET.	SD6A RET.	SD8B RET.	SD6B RET.
K	SC A RET.	SD7A RET.	SD 8 RET.	SD7B RET.
E	SC2A RET.	SD8A RET.	SD2B RET.	SD8B RET.
H	SD3A RET.	SD9A RET.	SD3B RET.	SD9B RET.
S	SC3A	SD8A	SD3B	SD8B
X	SD6A	SD6A	SD6B	SD6B
V	SD2A	SD8A	SD2B	SD8B
B	SD1A	SD7A	SD1B	SD7B
AA	SD12A	SD4A	SD12B	SD4B
W	SD11A	SD5A	SD11B	SD5B
5	PEC 0A	PEC 6A	PEC 0B	PEC 6B
6	PEC 3A	PEC 9A	PEC 3B	PEC 9B
7	PEC 11A	PEC 5A	PEC 11B	PEC 5B
8	PEC 2A	PEC 8A	PEC 2B	PEC 8B
9	PEC 12A	PEC 4A	PEC 12B	PEC 4B
10	PEC 1A	PEC 7A	PEC 1B	PEC 7B
	PEA	PEA2	PE B1	PE B2
12	PRB 12A	PRB 4A	PRB 12B	PRB 4B
13	SHIFT PRB 3A	SHIFT PRB 9A	SHIFT PRB 3B	SHIFT PRB 9B
14	PRB 1A	PRB 7A	PRB 1B	PRB 7B
15	SHIFT PRB 6A	SHIFT PRB 6A	SHIFT PRB 6B	SHIFT PRB 6B
16	PRB 2A	PRB 8A	PRB 2B	PRB 8B
19	SHIFT PRB 3A	CAMP	SHIFT PRB 3B	SHIFT PRB 9B
20	PRB 11A	PRB 8A	PRB 11B	PRB 2B
21	SHIFT PRB 6A	SHIFT PRB 6A	SHIFT PRB 6B	SHIFT PRB 6B
22	PRB A	PRB "A"	PRB B	PRB "B"
23	SHIFT A	SHIFT A	SHIFT B	SHIFT B

SEE SEPARATE PL

GENERAL DYNAMICS Electronics Division ROCHESTER N.Y.

E 58189

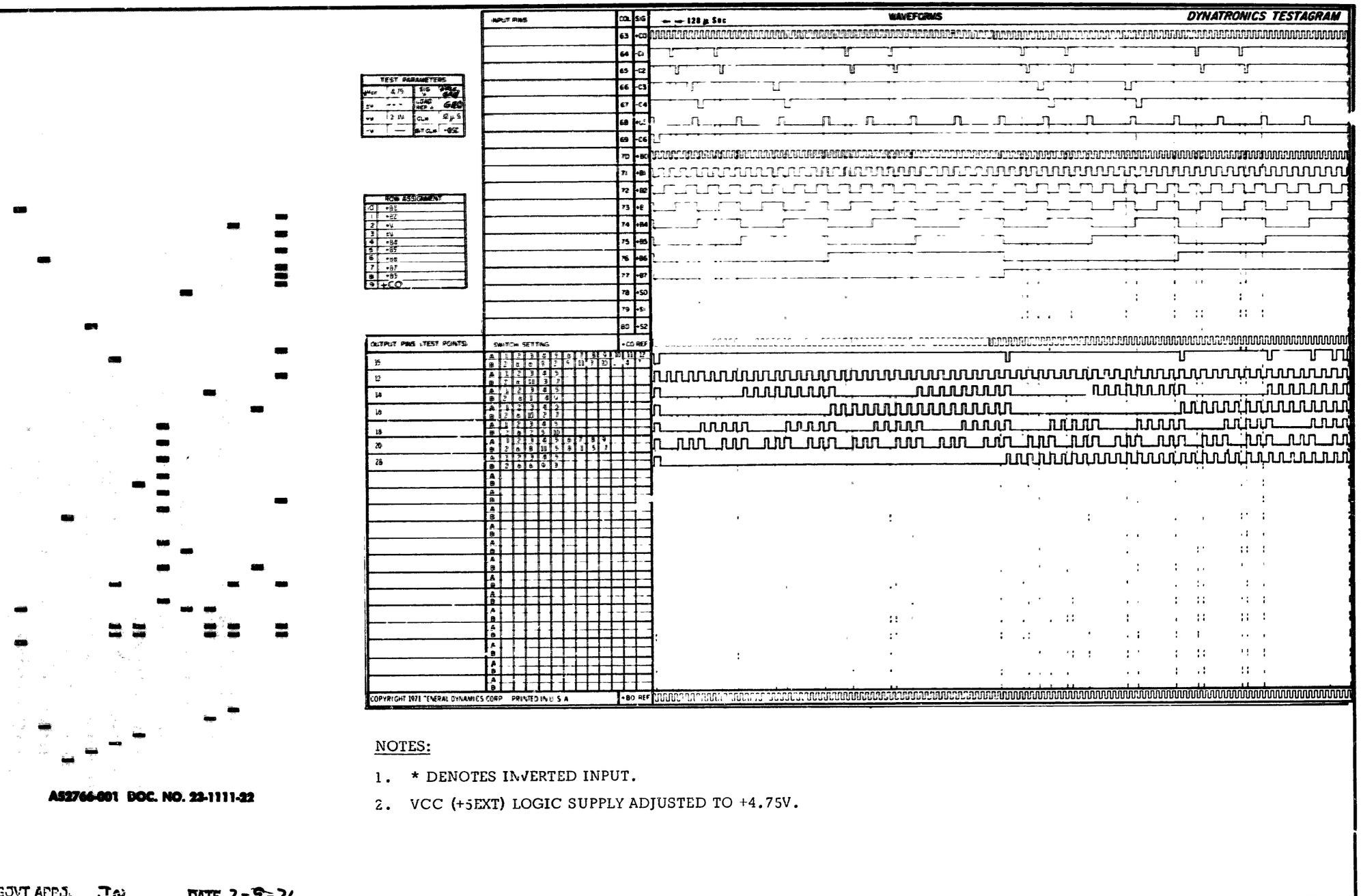
7-9-71

JN

P.C. Assembly A52766-001

P.C. Logic A52765

Doc. No. 23-1111-22

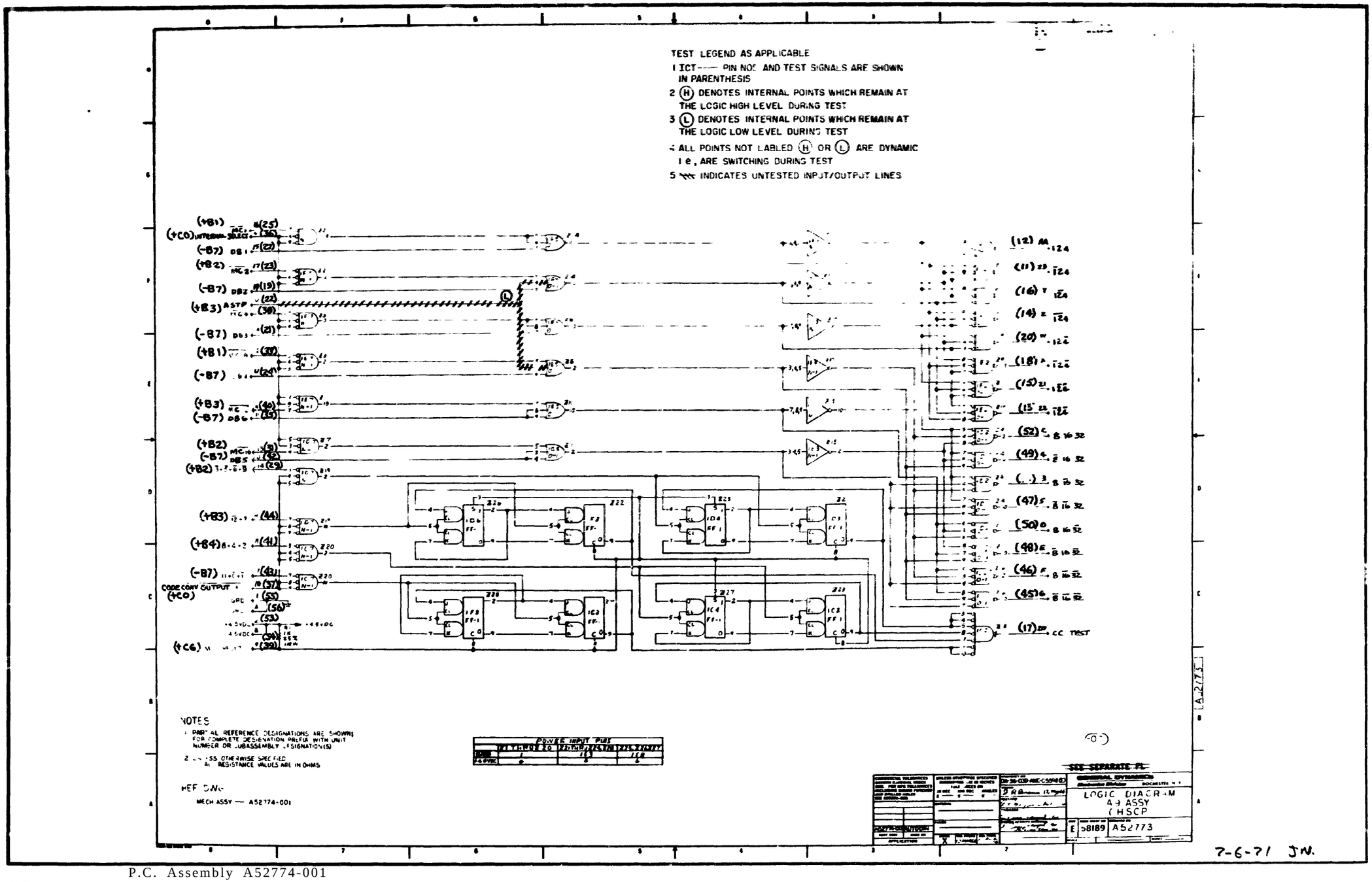


A52766-001 DOC. NO. 23-1111-22

NOTES:

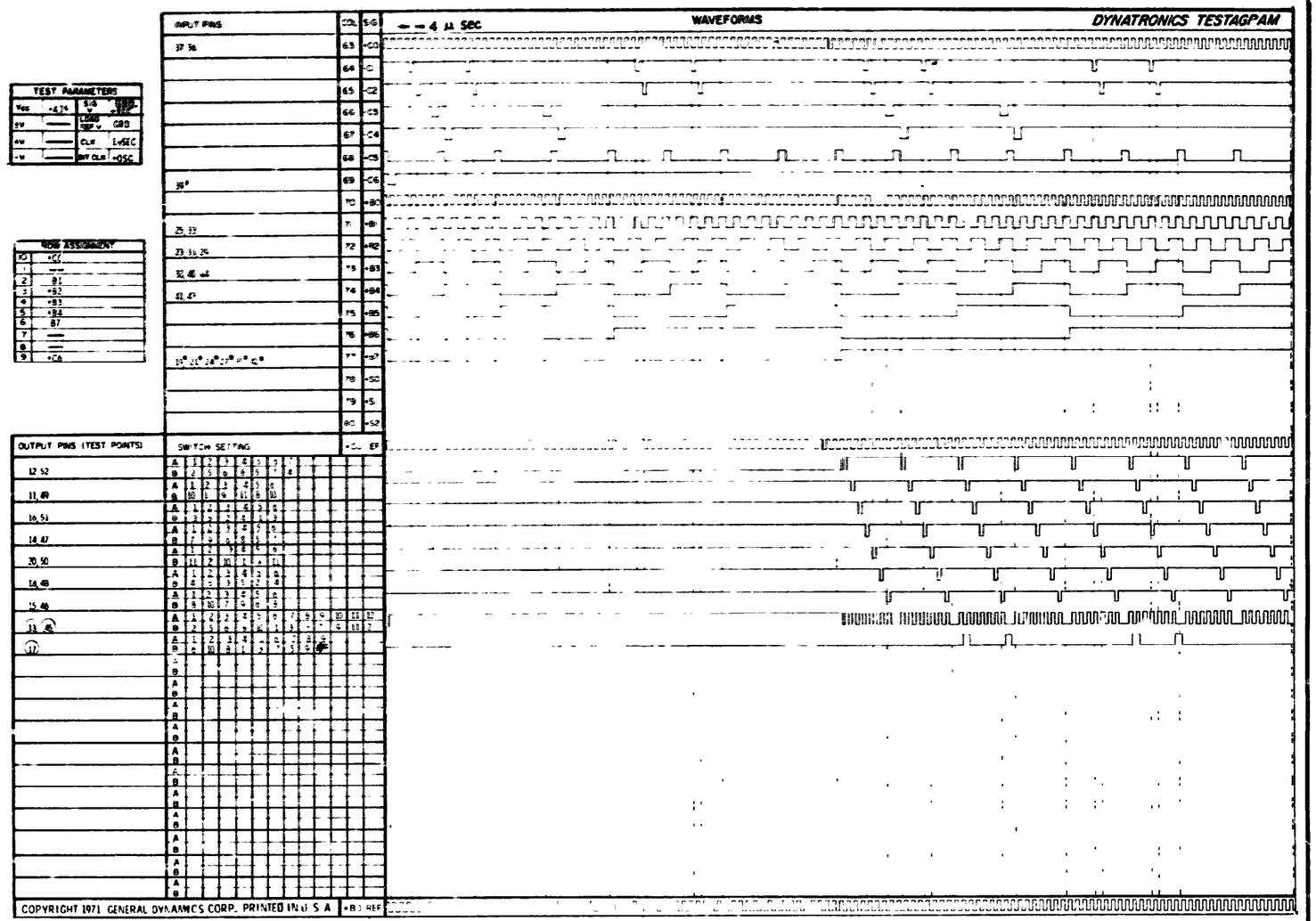
1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

GOVT APPD. JW DATE 7-9-71



P.C. Assembly A52774-001

P.C. Logic A52773



NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

A52774-001 DOC. NO. 23-1112-11

2-6-71 JN

TEST LEGEND AS APPLICABLE

1 LOT——PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

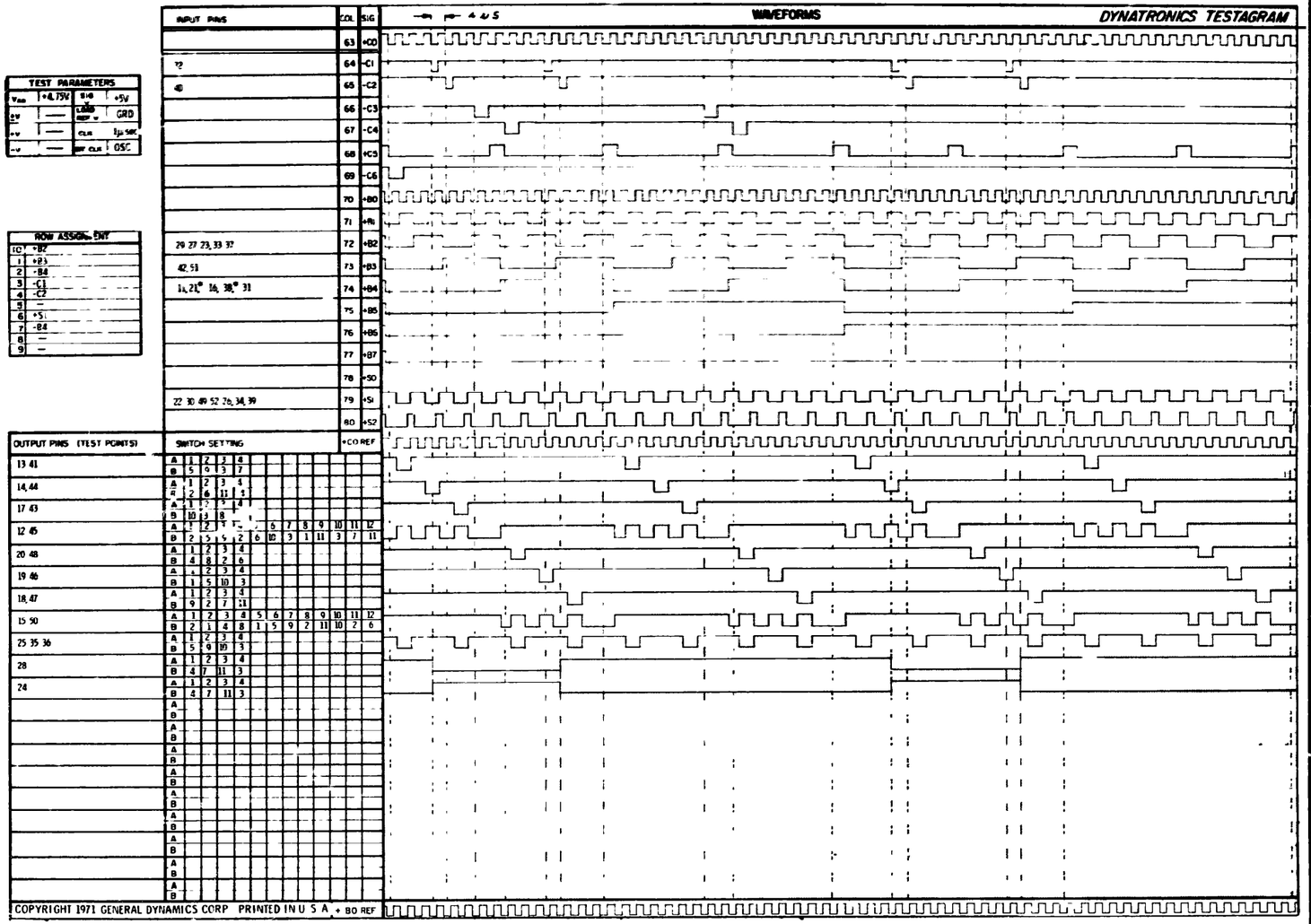
5 ⟿ INDICATES UNTESTED INPUT/OUTPUT LINES

7-9-71

JN

P.C. Assembly A53418-001

P.C. Logic A53417

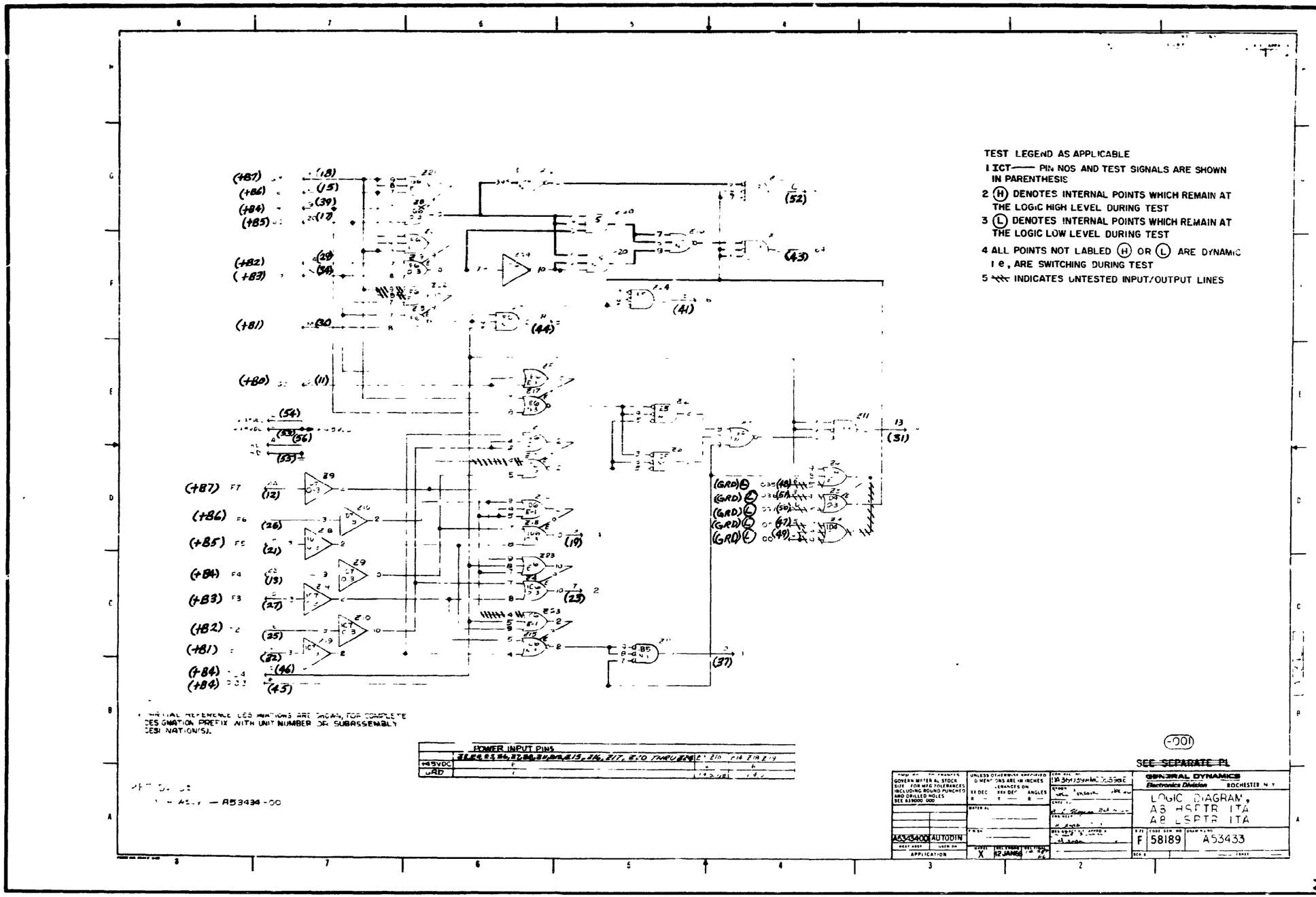


NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

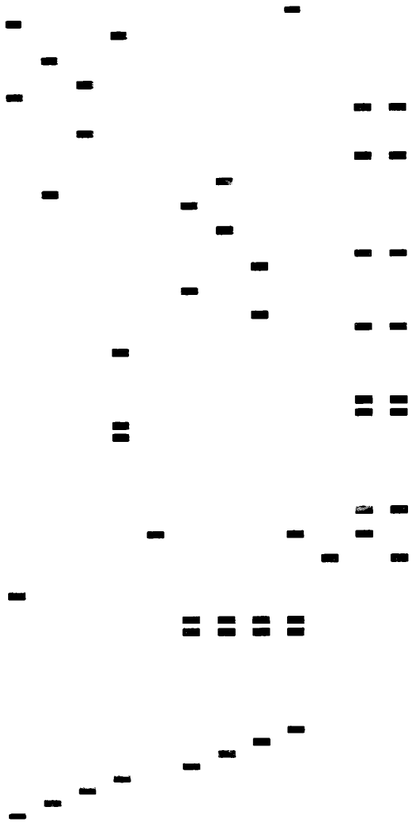
A53418-001 DOC. NO. 23-1113-11

GOVT APPD. JN DATE 7-9-71



P.C. Assembly A53434-001

P.C. Logic A53433 Doc. No. 23-1114-11



A53434-001 DOC. NO. 23-1114-11

7-6-71 JN

TEST PARAMETERS			
V_{CC}	4.75	SIG V	V
+V	—	LOAD REF V	GRD
+V	—	CLR	1 μ sec
-V	—	INT CLK	+ OSC

ROW ASSIGNMENT	
10	—
1	+B0
2	+B1
3	+B2
4	+B3
5	—
6	+B4
7	+B5
8	+B6
9	+B7

INPUT PINS	COL	SIG
85 .4	63	+C0
	64	C1
	65	C2
	66	-C3
	67	C4
	68	+C5
	69	-C6
11	7	+B0
32 36	71	+B1
25 29	72	+B2
27 34	73	+B3
1, 39 45 46	74	+B4
17 21	75	+B5
15 20	76	+B6
12 18	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
37 41	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 6 10 3 1 11 10 2 6 10 8 7 6
23	A 1 2 3 4 5 / B 2 10 11 8 #
19	A 1 2 3 / B 2 1 #
43	A 1 2 3 / B 2 1 #
41	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 10 1 8 10 9 8 7 6 5 4 3 2
52	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 11 10 9 8 7 6 5 4 3 2 1 11
31	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 2 4 8 10 1 3 5 7 11 1 11 2
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B

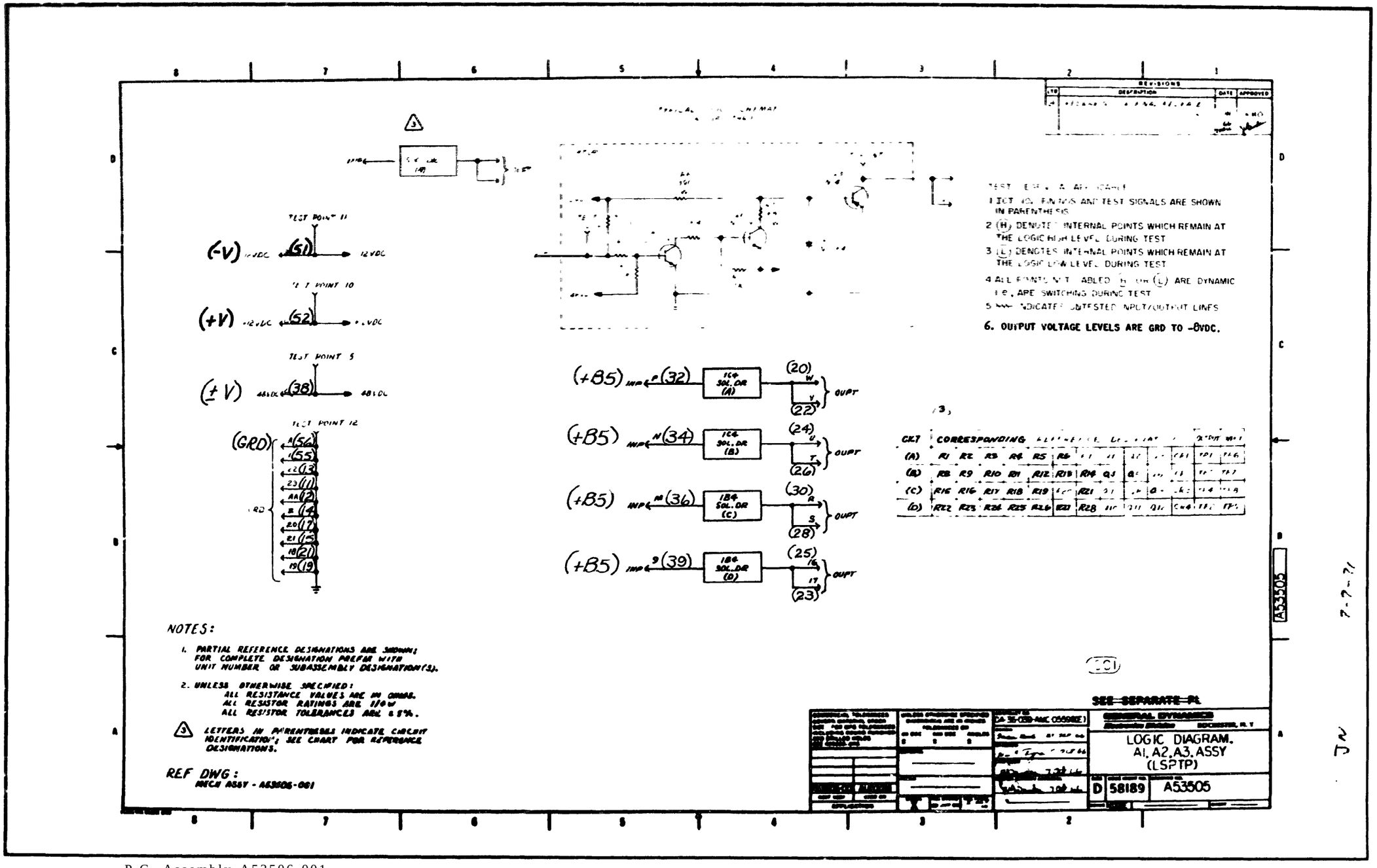
WAVEFORMS — ← → 4 μ SEC — DYNATRONICS TESTAGRAM

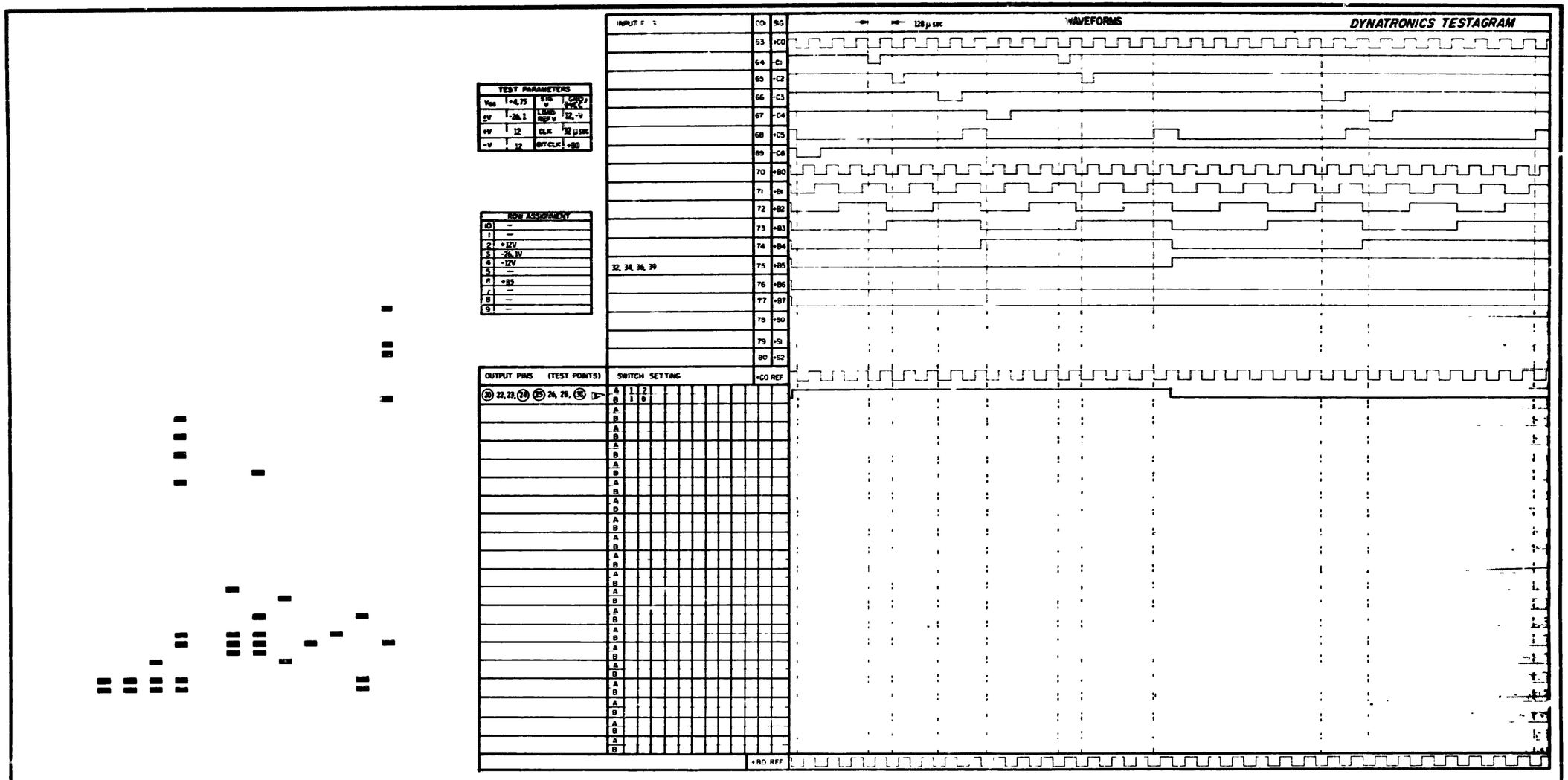
 +B0 REF

NOTES:

1. *DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH NO. 12 WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.


REVISIONS
DESCRIPTION
DATE
APPROVED
TEST POINT 11
(-V)
-12VDC
(51)
12VDC
TEST POINT 10
(+V)
+12VDC
(52)
+5VDC
TEST POINT 5
(± V)
48VDC
(38)
48VDC
TEST POINT 12
(GRD)
GRD
(56)
(55)
(13)
(11)
(12)
(14)
(17)
(15)
(21)
(19)
(+B5)
(32)
IC# SOL. DR (A)
(20)
(22)
OUPT
(34)
IC# SOL. DR (B)
(24)
(26)
(36)
IB# SOL. DR (C)
(30)
(28)
(39)
IB# SOL. DR (D)
(25)
(23)
TEST CONDITIONS & APPLICABLE
1 TEST VOLTAGES AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST
5 INDICATES UNTESTED INPUT/OUTPUT LINES
6. OUTPUT VOLTAGE LEVELS ARE GRD TO -8VDC.
CKT
CORRESPONDING
(A) R1 R2 R3 R4 R5 R6
(B) R8 R9 R10 R11 R12 R13 R14
(C) R15 R16 R17 R18 R19
(D) R22 R23 R24 R25 R26 R27 R28
NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
2. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE VALUES ARE IN OHMS.
ALL RESISTOR RATINGS ARE 1/10W
ALL RESISTOR TOLERANCES ARE ± 5%.
3 LETTERS IN PARENTHESES INDICATE CIRCUIT IDENTIFICATION; SEE CHART FOR REFERENCE DESIGNATIONS.
REF DWG:
MECH ASSY - A53506-001
SEE SEPARATE PL
GENERAL DYNAMICS
LOGIC DIAGRAM. A1, A2, A3, ASSY (LSPTP)
D
58189
A53505
A53505
7-7-71



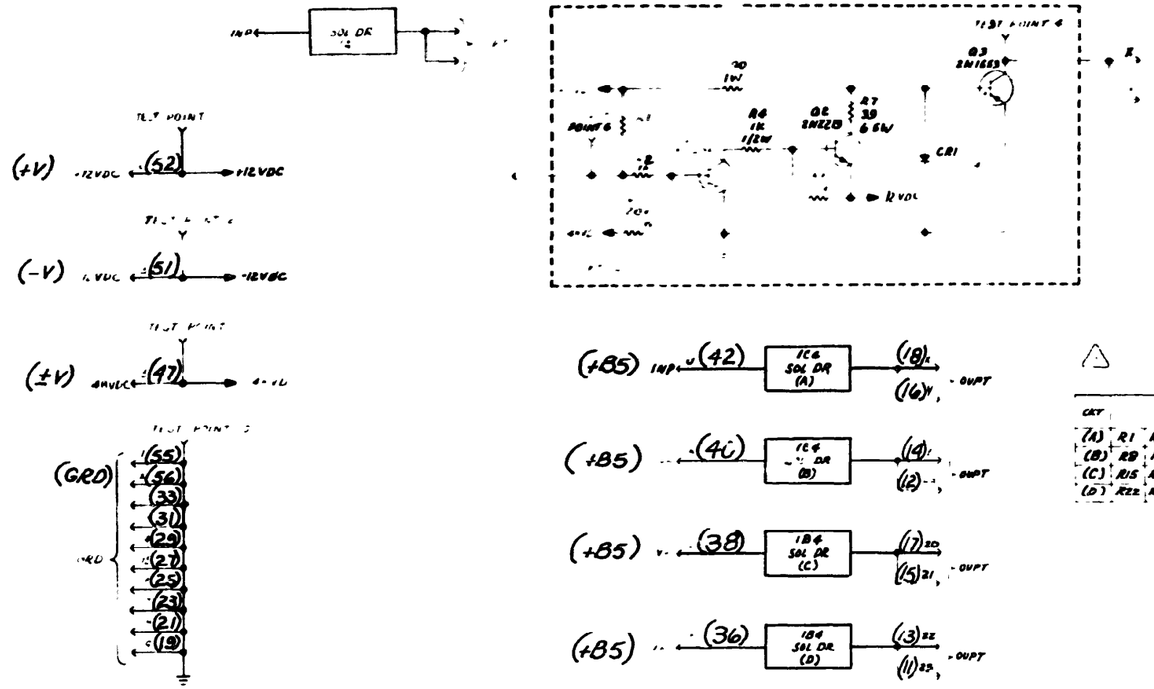
NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
3. OUTPUT VOLTAGE LEVELS ARE GRD TO -8VDC APPROX.

TYPICAL LOGIC / SCHEMATIC
CKTS (A) THRU (D)

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED



TEST LEGEND AS APPLICABLE

1 ICT- 02 PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

5 ≈≈ INDICATES UNTESTED INPUT/OUTPUT LINES

6. OUTPUT VOLTAGE LEVELS ARE GRD TO -8VDC APPROX.

CKT	CORRESPONDING REFERENCE DESIGNATIONS												INPUT	OUTPUT
(A)	R1	R2	R3	R4	R5	R6	R7	CR1	Q1	Q2	Q3	TP6		TP4
(B)	R8	R9	R10	R11	R12	R13	R14	CR2	Q4	Q5	Q6	TP7		TP1
(C)	R15	R16	R17	R18	R19	R20	R21	CR3	Q7	Q8	Q9	TP8		TP3
(D)	R22	R23	R24	R25	R26	R27	R28	CR4	Q10	Q11	Q12	TP5		TP2

NOTES:

ALL INITIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION.

UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE VALUES ARE IN OHMS.
ALL RESISTOR RATINGS ARE 1/4 W.
ALL RESISTOR TOLERANCE ARE ± %.

3 LETTERS IN PARENTHESES INDICATE CIRCUIT IDENTIFICATION SEE CHART FOR REFERENCE DESIGNATIONS

REF DWG:

MECH ASSY A53510-001

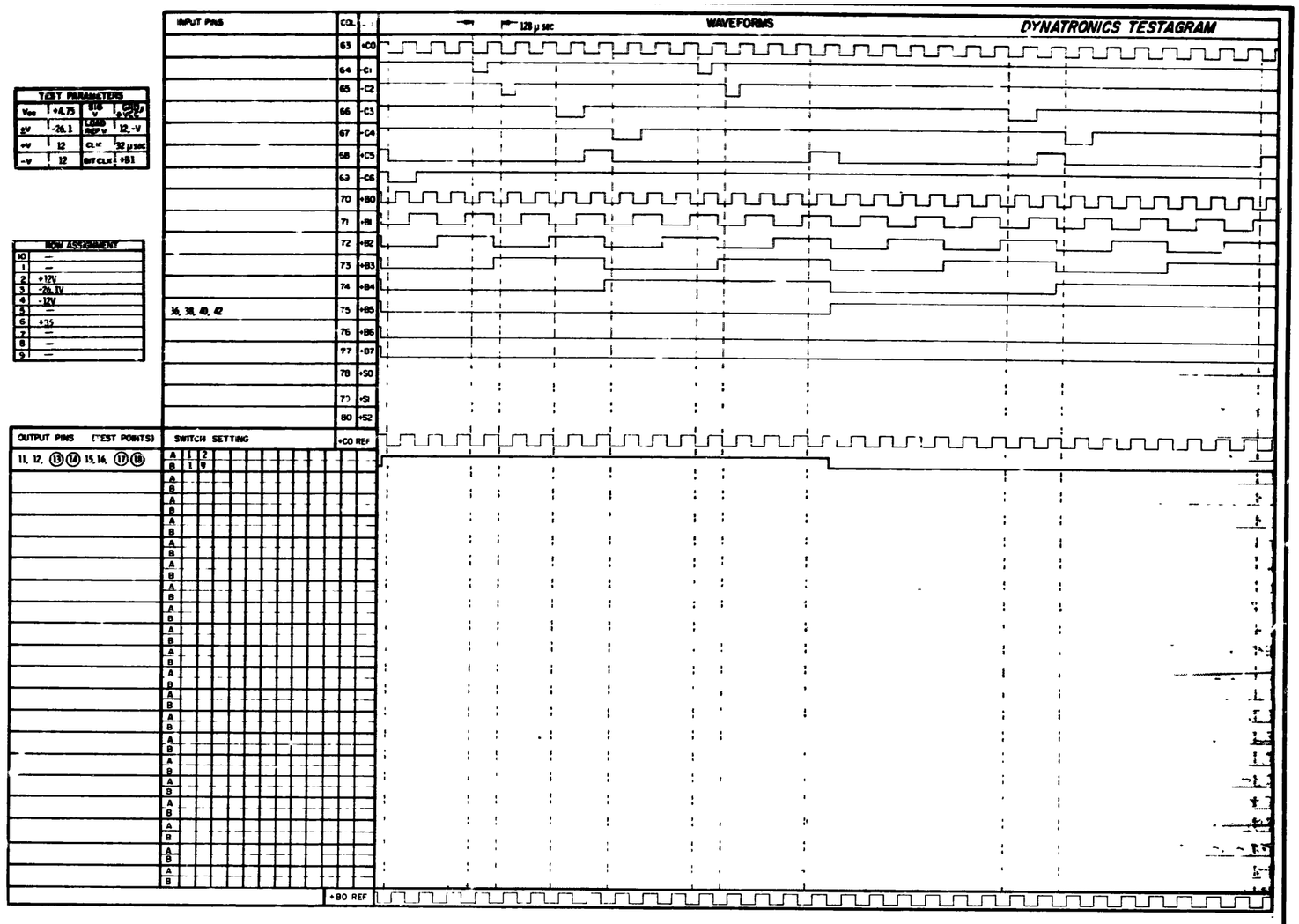
(-001)

SEE SEPARATE PL

COMMERCIAL TOLERANCES GOVERN MATERIAL STOCK SIZE FOR MFG TOLERANCES INCLUDING ROUND PUNCHED AND DRILLED HOLES SEE S3900B-000	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON XX DEC ± — XXX DEC ± — ANGLES ± —	CONTRACT NO DA 36-039 AMC 05598(E)	GENERAL DYNAMICS Electronics Division ROCHESTER, N Y
		DRAWN Jean Bush 27 Sept 66	LOGIC DIAGRAM A1, A2, A3, ASSY (HSPTP)
		ENGINEER 1 OCT 66	
		PROJECT ENGR	
		DESIGN ACTIVITY APPROVAL	SIZE D CODE IDENT NO 58189 DRAWING NO A53509
A53510-001 AUTODIN			SCALE NONE SHEET
NEXT ASSY APPLICATION	USED ON		

A53509

DATE 7-7-71



NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
3. OUTPUT VOLTAGE LEVELS ARE GRD TO -8VDC APPROX.

A53510-001 DOC. NO. 23-2190-11

GOVT APPD. JN DATE 7-7-71

TEST LEGEND AS APPLICABLE

1 ICT- — PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES

DIVISIONS			
APPD	NO	DESCRIPTION	DATE APPROVED
	A	RELEASED FOR FINAL RELEASE	
	B	REV PER ECN 5201-1776 JB	

CCR INPUT PINS		
PINS	HSCII MODE	ITA #2 MODE
V	RCH	RCH
U	1	—
A	2	—
J		1
H	4	—
23		2
L	8	—
22		4
M	16	—
21		8
P	32	—
S		16
E	64	—
U	128	—
19	DI	DI
2	NDI	NDI
6	LSEL	CSEL
B	—	—
5	—	—
7	—	—
9	—	—
11	—	—
13	—	—
14	—	—
17	—	—

CCR OUTPUT PINS		
PINS	HSCII MODE	ITA #2 MODE
RR	4	2
V	8	3
J	16	6
N	32	16
K	64	—
T	128	—
20	DI	DI
1	NDI	NDI
4	PI NADV RST	PI NADV RST
H	BSP	BSP
4	PI ADV RST	PI ADV RST
2	NBSP	NBSP
C	1	—
E	2	T

POWER INPUT PINS	
	12,22,24,23,29,210,211, 214 THRU 246
4.5VDC	6
GRD	1

NOTES:

1. SIGNAL REFERENCE DESIGNATIONS ARE SHOWN FOR CONN "A" OF CONNECTOR ZA53 A WITH UNIT NUMBER AS PREFIX. (i.e. CHARTONISL)
2. N.I. = INVERTER SPECIFIED
3. ALL RESISTOR VALUES ARE IN OHMS

REF DWG:
MFGNAV AR MFGEMBLY — A53584 001

(001)

~~SEE SEPARATE PL~~

COMMERCIAL TOLERANCES GOVERN MATERIAL STOCK SIZE FOR MFG TOLERANCES INCLUDING ROUND PUNCHED AND DRILLED HOLES REF ANSDM 000

UNLESS OTHERWISE SPECIFIED DIMENS ONS ARE IN INCHES TOLERANCES ON .XX DEC .XXX DEC ANGLES

A53584 V CAUTION

APPLICATION

DA-36-039 AMC 05598(E)

GENERAL DYNAMICS
Electronics Division ROCHESTER N Y

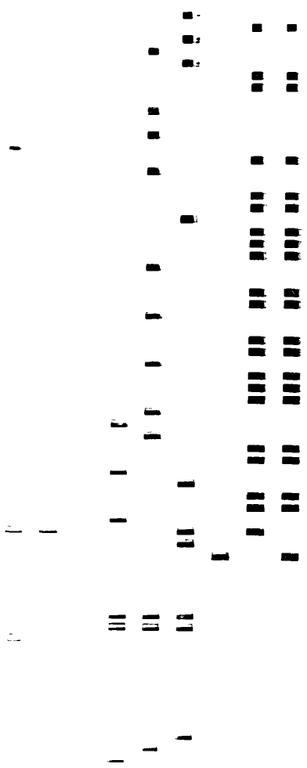
LOGIC DIAGRAM, A12 ASSEMBLY (H/LSPTP)

F 58189 A53583

A53583

7-9-71

JW



A53584-001 DOC. NO. 23-2107-11

GOVT APPD. JN. DATE 7-6-71

TEST PARAMETERS

V_{BB}	+4.5V	SIG GEN	+4.5V
0V		LOAD REF V	GRD
+V		CLK	1 μsec
-V		CLK	+OSC

ROW ASSIGNMENT

10	—
1	+B1
2	+B2
3	+B3
4	—
5	—
6	-CO
7	—
8	—
9	—

INPUT PINS	COL	SIG
22 NF	63	+CO
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+BO
11, 13, 15 28, 50 55	71	+B1
14, 19 21 24, 32 36, 40 44, 46	72	+B2
45 49 53	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+SO
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS) — SWITCH SETTING — +CO REF

(18)
(17)
(52)
(12) (34) (38) (47) (48)
(26) (30)
(29) 41
51
31 35 39 43 47
23 27

+BO REF

WAVEFORMS — 4 μ SEC — DYNATRONICS TESTAGRAM

NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
3. * DENOTES INVERTED SIGNAL.

TEST LEGEND AS APPLICABLE

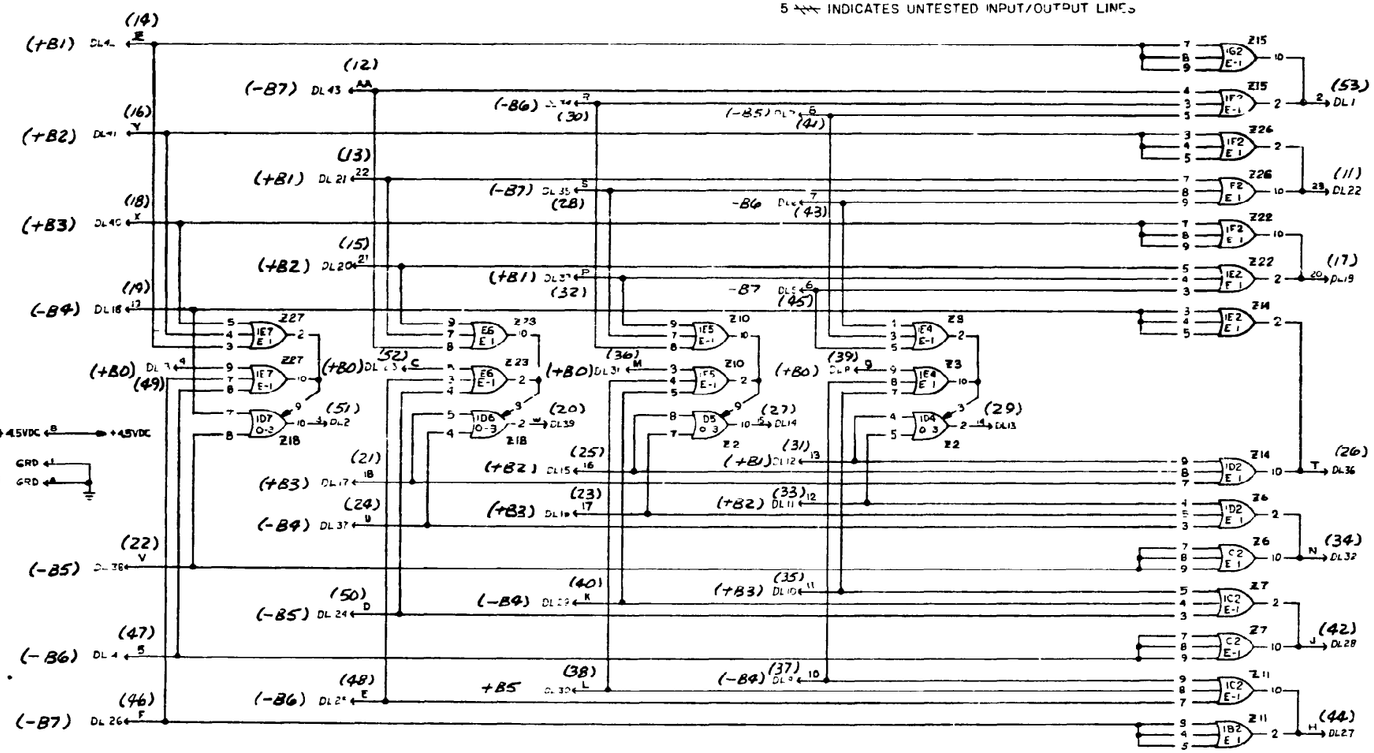
1 ICT- PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e , ARE SWITCHING DURING TEST

5 ~~xxx~~ INDICATES UNTESTED INPUT/OUTPUT LINES



NOTES:

1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION ISL

	POWER INPUT PINS
	Z2 Z3 Z6 Z7 Z9 Z11 Z14 Z15 Z18 Z22 Z23 Z26 Z27
GRD	1
+4.5VDC	6

REF DWG:

MECH ASSY - A53721-001

(-001)

SEE SEPARATE PL

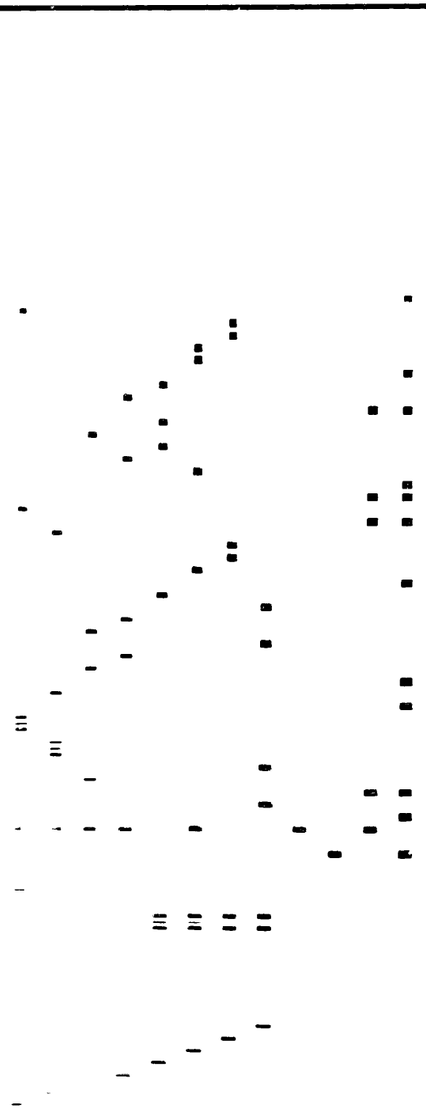
GENERAL DYNAMICS
Electronics Division ROCHESTER N Y

LOGIC DIAGRAM, ENCODE MATRIX

F 58189 A53720

A53720

7-6-71



A53721-001 DOC. NO. 23-2108-11

GOVT APPD. JW DATE 7-6-71

TEST PARAMETERS

Vcc	+4.75V	SIG V	0/VCC
±V	——	LOAD REF V	GRD
+V	——	CLK	2μ sec
-V	——	BIT CLK	+OSC

ROW ASSIGNMENT

10	—
1	—
2	+B0
3	+B1
4	+B2
5	+B3
6	B4
7	B5
8	B6
9	B7

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
36 39 49 52	70	+B0
13 14, 31 32	71	+B1
15 16 25 33	72	+B2
18 21. 23 35	73	+B3
19 24 37* 40*	74	+B4
22 38* 41* 50*	75	+B5
30* 43 47* 48*	76	+B6
12* 28* 45* 46*	77	+B7
	78	+S0
	79	+S1
	80	+S2
SWITCH SETTING		+CO REF

OUTPUT PINS (TEST POINTS)

20 27 29 51

44 42 34 36 17 11 13

WAVEFORMS — 8μ sec

DYNATRONICS TESTAGRAM

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

TEST LEGEND AS APPLICABLE

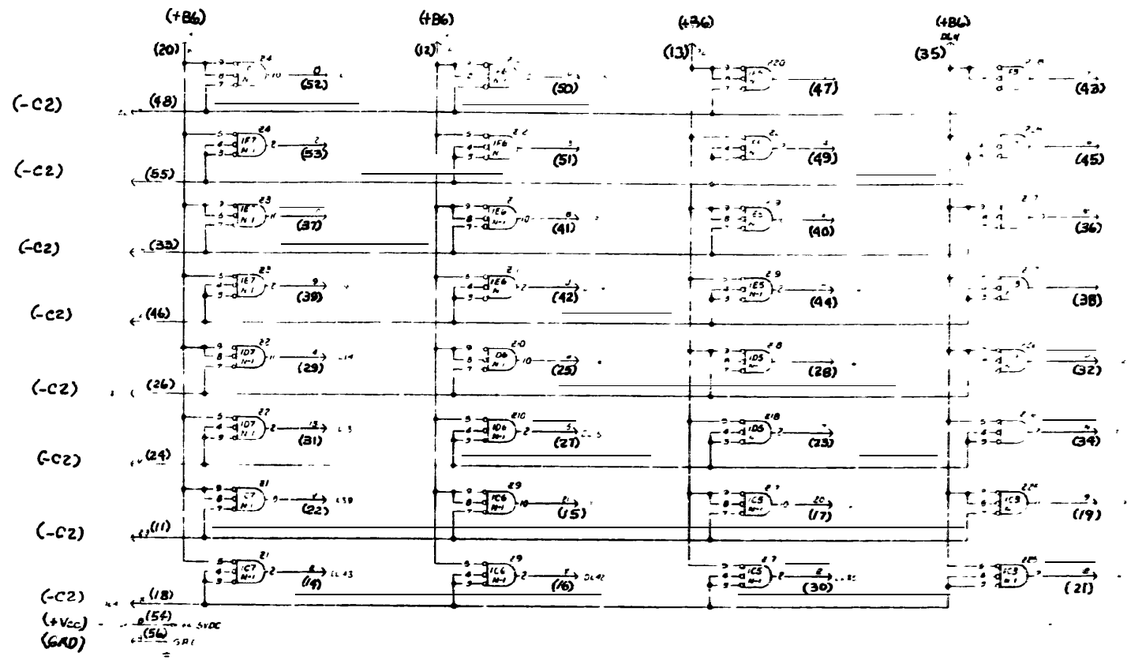
1 ICT—— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES



NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN
2. COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER
3. ASSEMBLY DESIGNATION (S)

REF DWG

ASSY — A53725-001

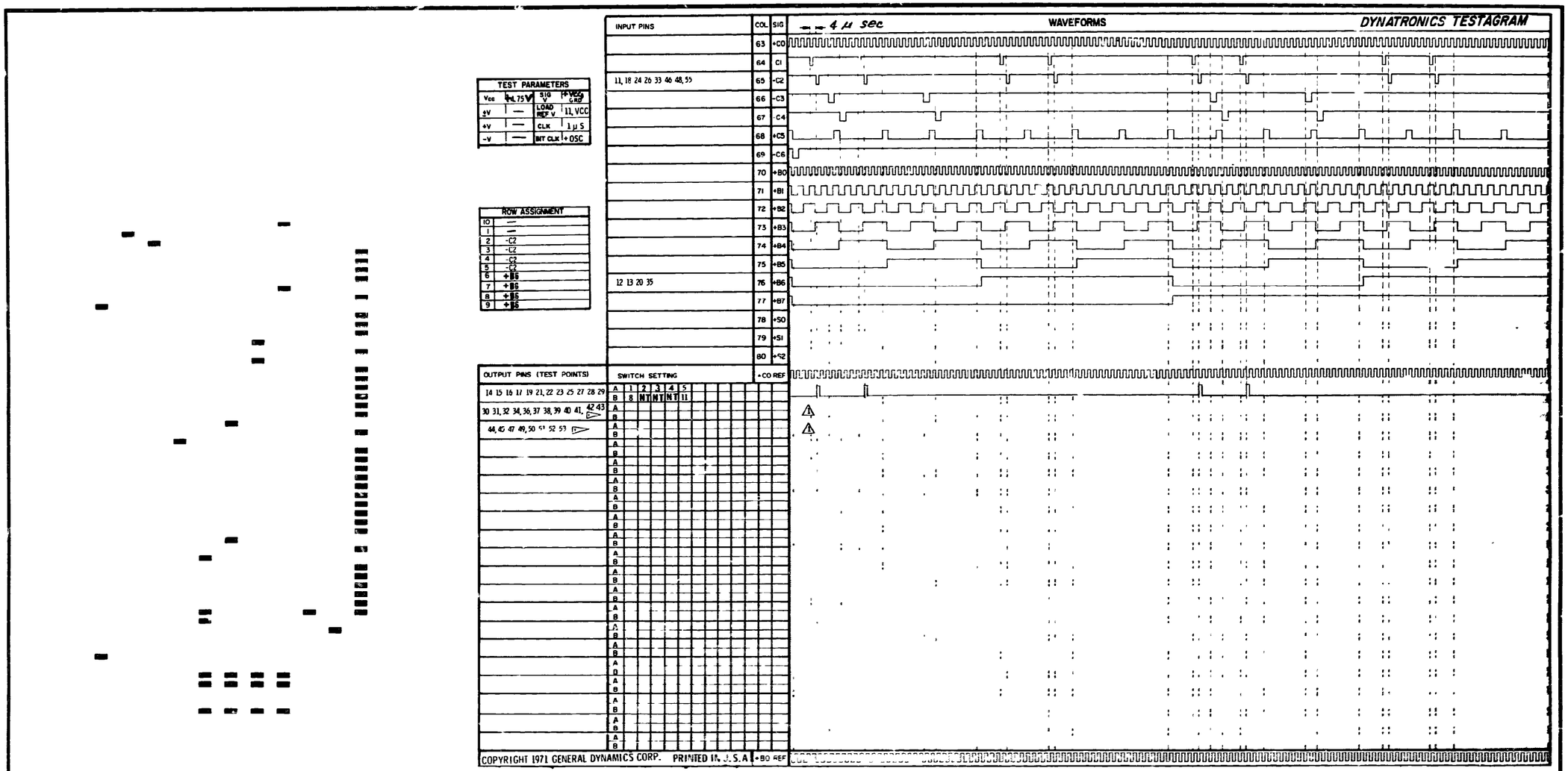
SEE SEPARATE PL

GENERAL DYNAMICS

LOGIC DIAGRAM,

E 58189 A53725

7-6-21

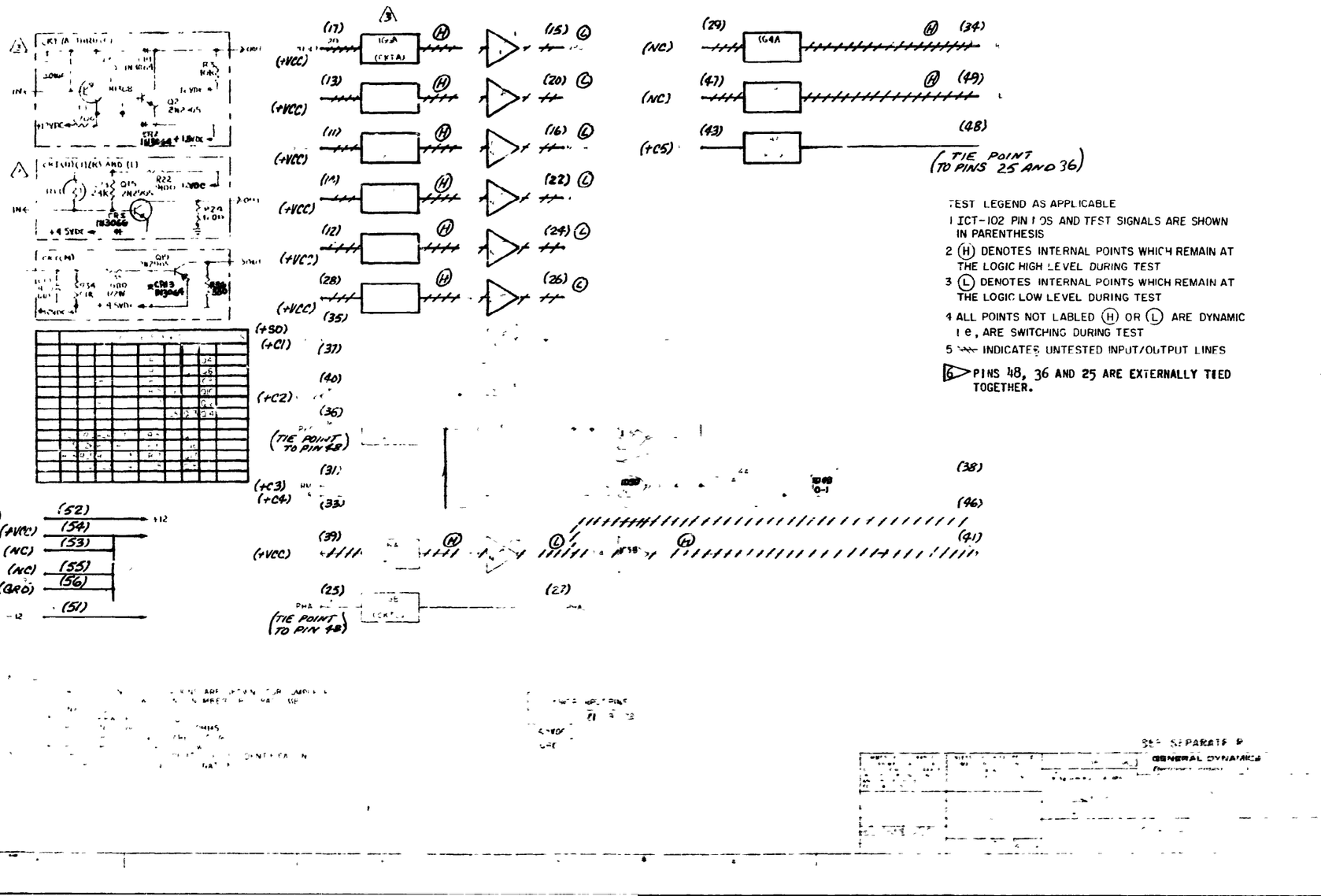


A53725-001 DOC. NO. 23-2109-11

GOVT APPD. JN DATE 2-6-71

NOTES:

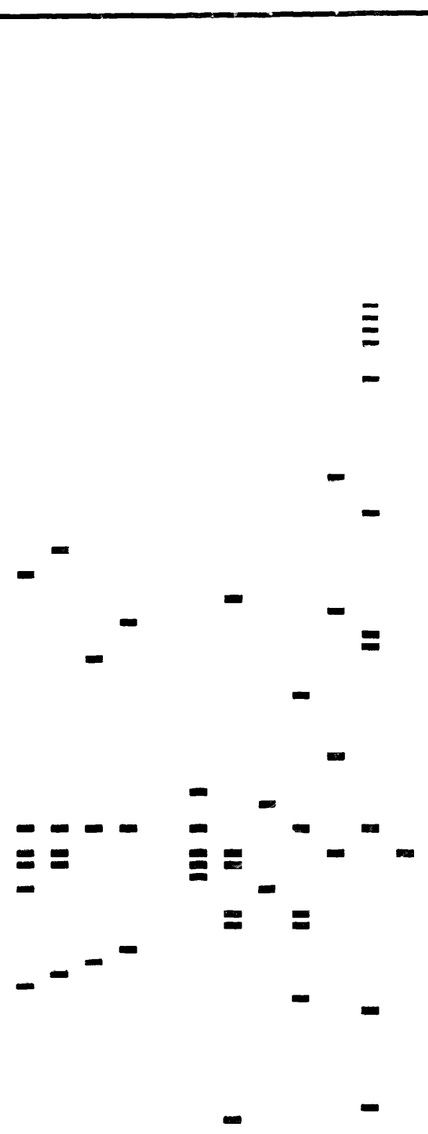
1. WAVEFORMS AND A,B SWITCH POSITIONS IDENTICAL FOR ALL OUTPUTS.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO 4.75V.
3. NT INDICATES NO TEST.



P.C. Assembly A65111-011

P.C. Form A65999

Doc. No. 2[illegible]-1

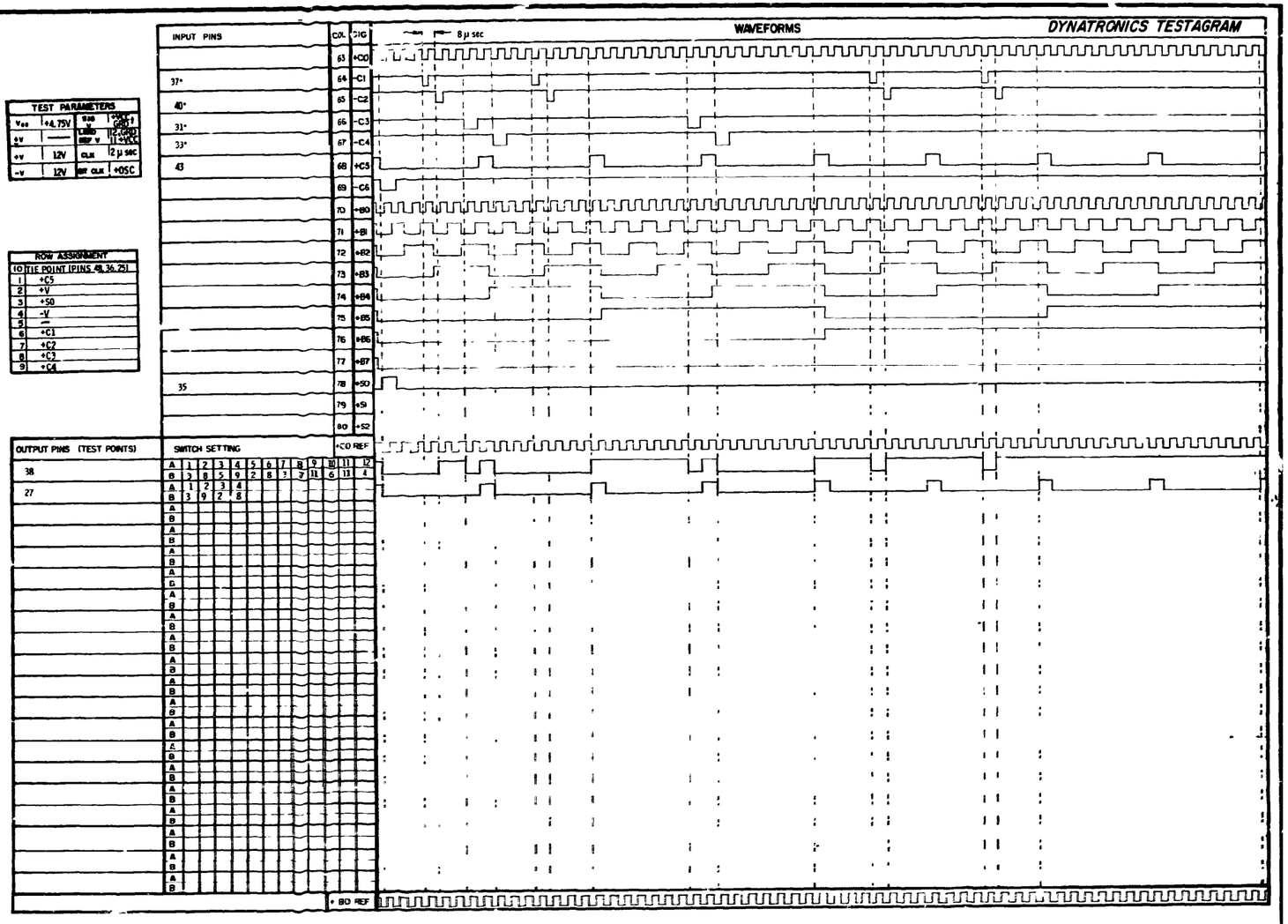


A65001-001 DOC. NO. 23-2110-11

GOVT APPD. JN DATE 7-6-71

TEST PARAMETERS			
V_{DD}	+4.75V	SYNC	8 μ sec
-V	——	DATA	1 μ sec
+V	12V	CLK	2 μ sec
-V	12V	REF CLK	+OSC

ROW ASSIGNMENT	
10	TIE POINT (PINS 48, 36, 25)
1	+C5
2	+V
3	+S0
4	-V
5	—
6	+C1
7	+C2
8	+C3
9	+C4



NOTE:

1. * DENOTES INVERTED SIGNAL.

TEST LEGEND AS APPLICABLE

1 ICT—— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

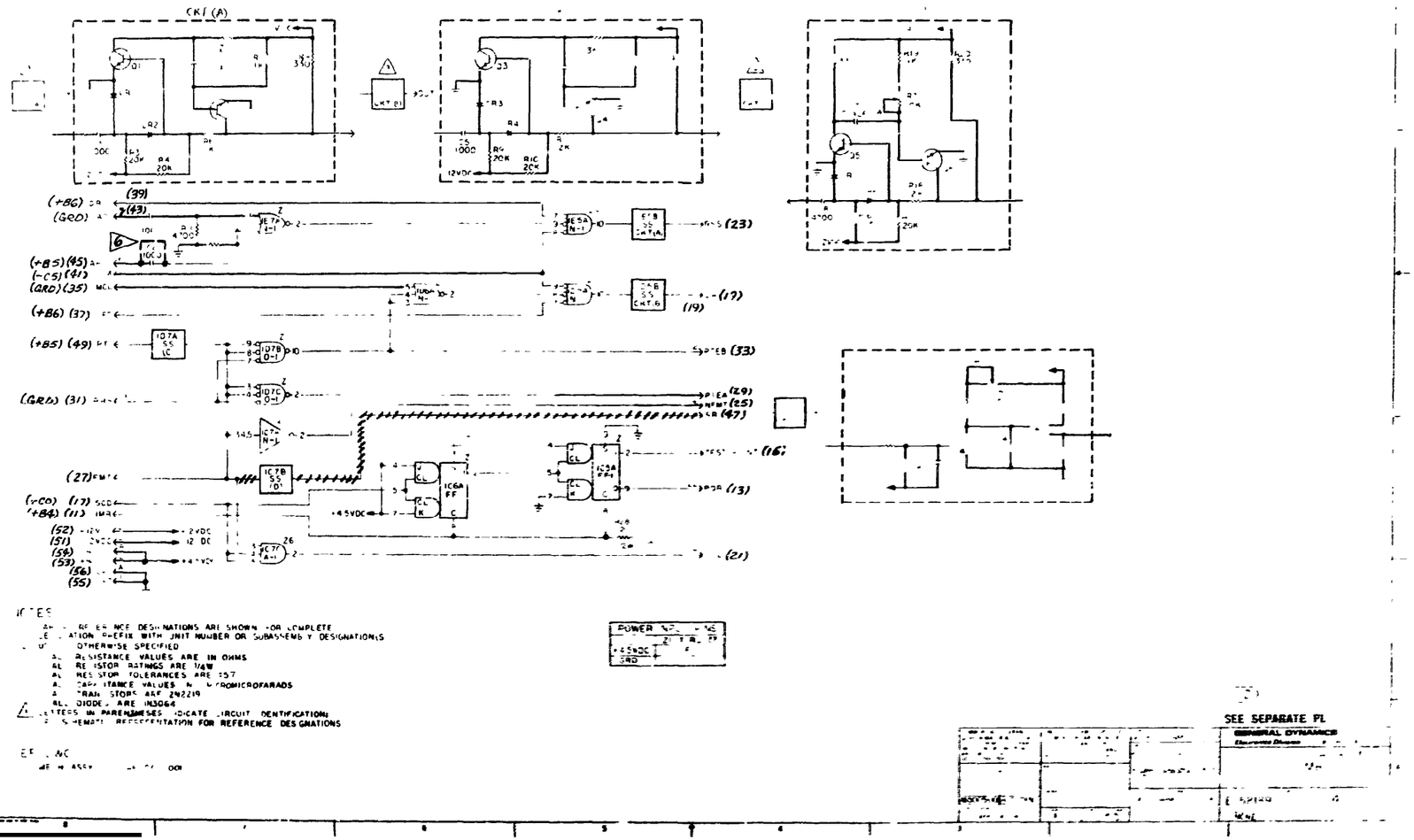
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

5 ⫽ INDICATES UNTESTED INPUT/OUTPUT LINES

CAPACITOR C2 JUMPERED DURING TEST.



NOTES

A1 REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATIONS

A2 UNLESS OTHERWISE SPECIFIED

A3 RESISTANCE VALUES ARE IN OHMS

A4 RESISTOR RATINGS ARE 1/4W

A5 RESISTOR TOLERANCES ARE ±5%

A6 CAPACITANCE VALUES ARE IN MICROMICROFARADS

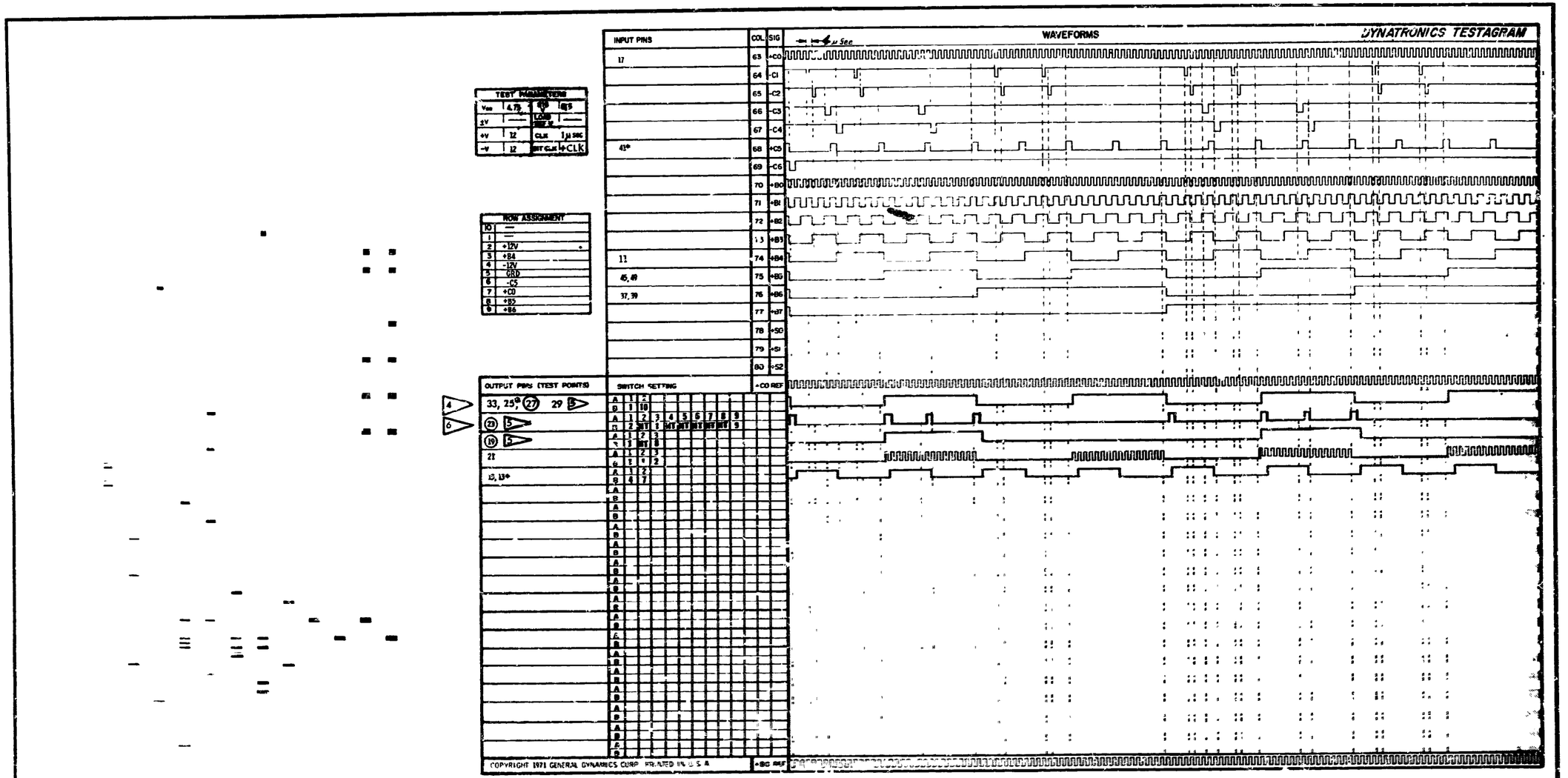
A7 TRANSISTORS ARE 2N2219

A8 ALL DIODES ARE IN3064

⚠ LETTERS IN PARENTHESES INDICATE CIRCUIT IDENTIFICATION

2 SCHEMATIC REPRESENTATION FOR REFERENCE DESIGNATIONS

REFERENCE ASSY

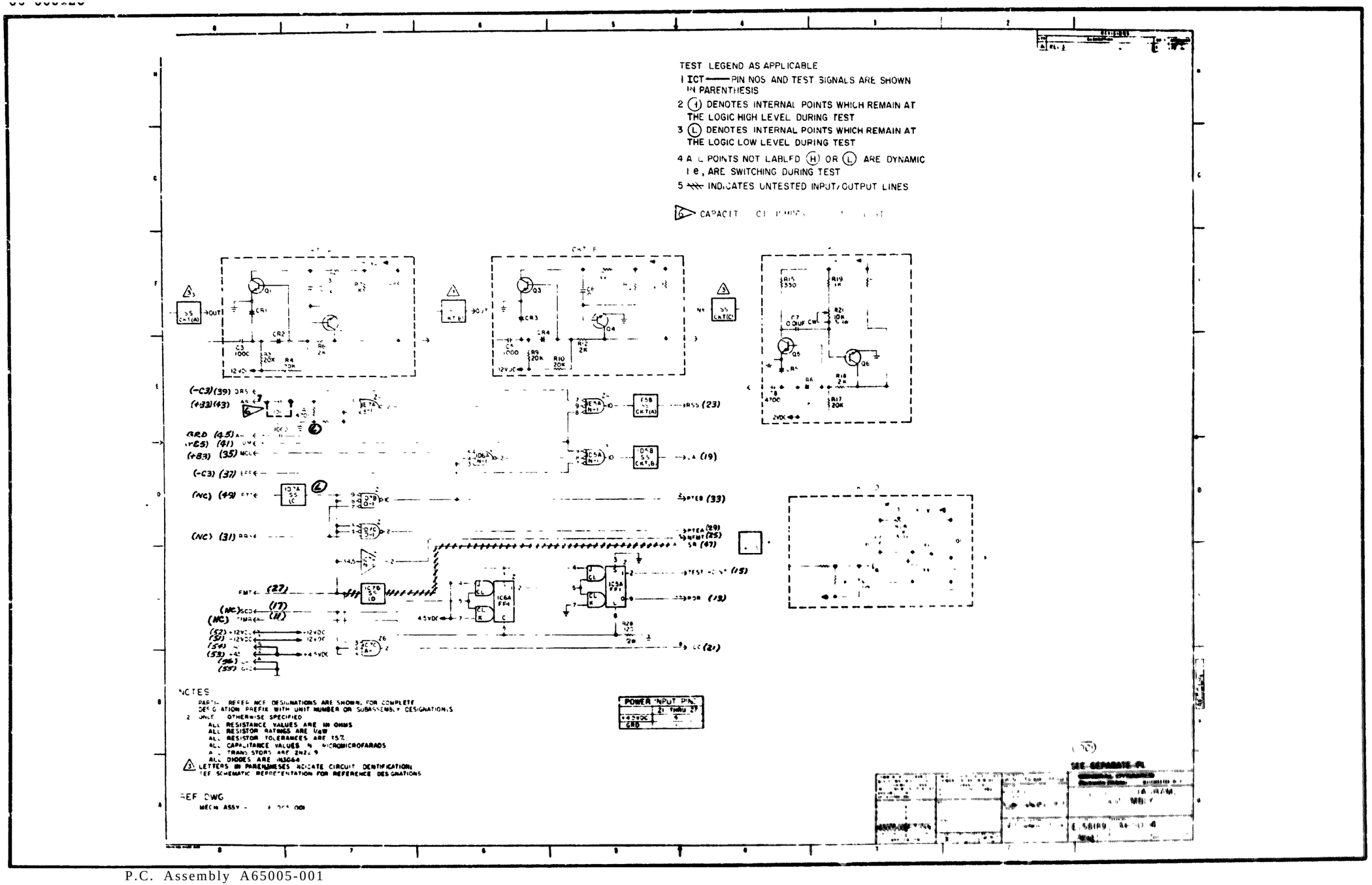


NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. BEFORE PROCEEDING WITH TEST, SELECT PIN 33 AND ADJUST R21 FOR A "GO" AT SWITCH SETTINGS A-1,B-1 AND A-2,B-10.
5. ALL "B" SWITCH SETTINGS MAY OCCUR ±1 "B" SWITCH SETTING FROM SETTINGS SHOWN.
6. PLACE A JUMPER ACROSS CAPACITOR C2 PRIOR TO TESTING P.C. CARD.
7. NT INDICATES NO TEST.

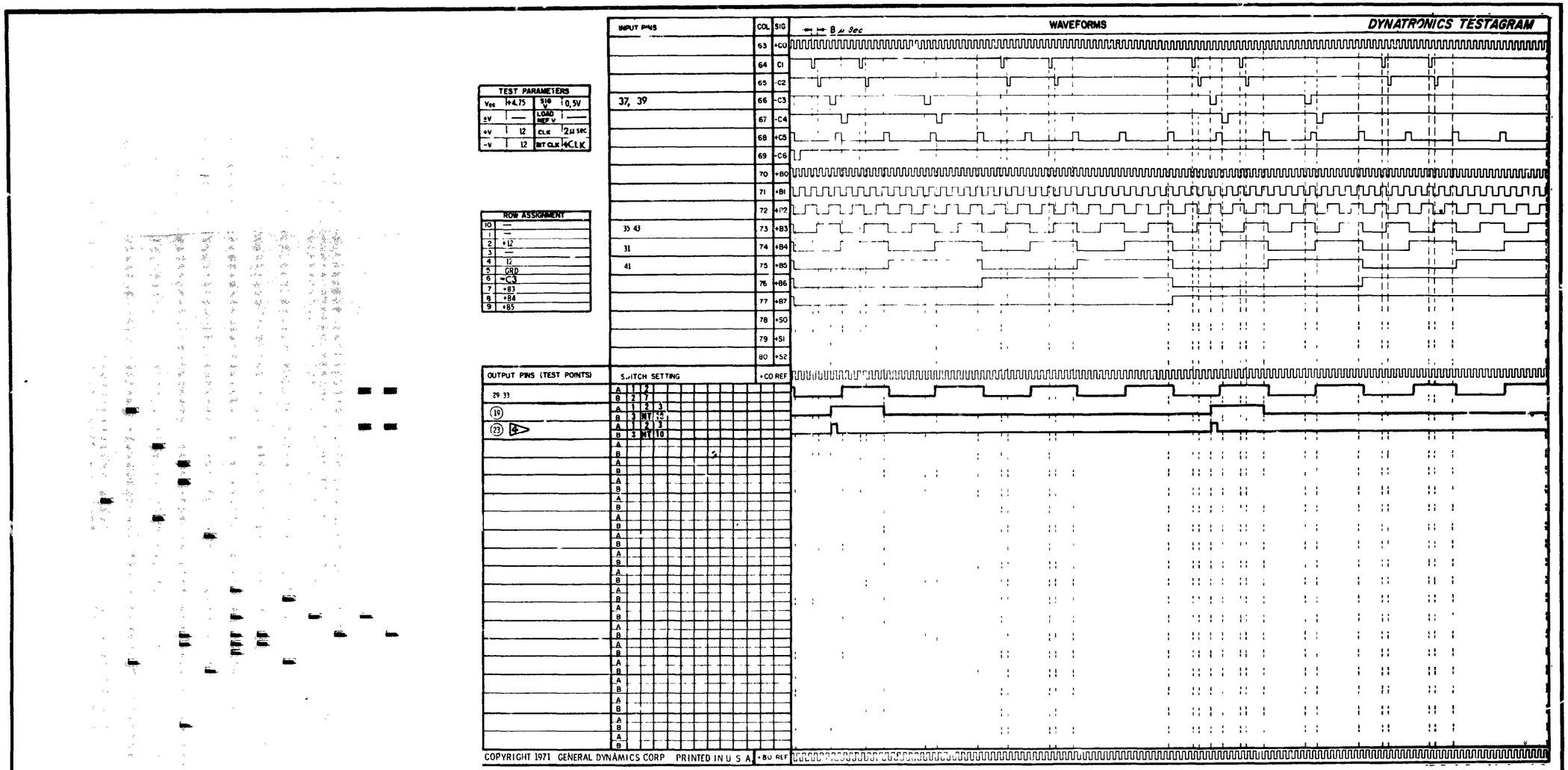
A65005 DOC. NO. 23-1119-12

GVT APPD. JW DATE 7-9-71



P.C. Assembly A65005-001

P.C. Logic A65004



A65005 DOC. NO. 23-1119-22

GOVT APPD. JN DATE 7-9-71

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. PLACE A JUMPER ACROSS CAPACITOR C1 PRIOR TO TESTING.
5. NT INDICATES NO TEST.

GOVT APPD. JN DATE 8-19-71

TEST LEGEND AS APPLICABLE

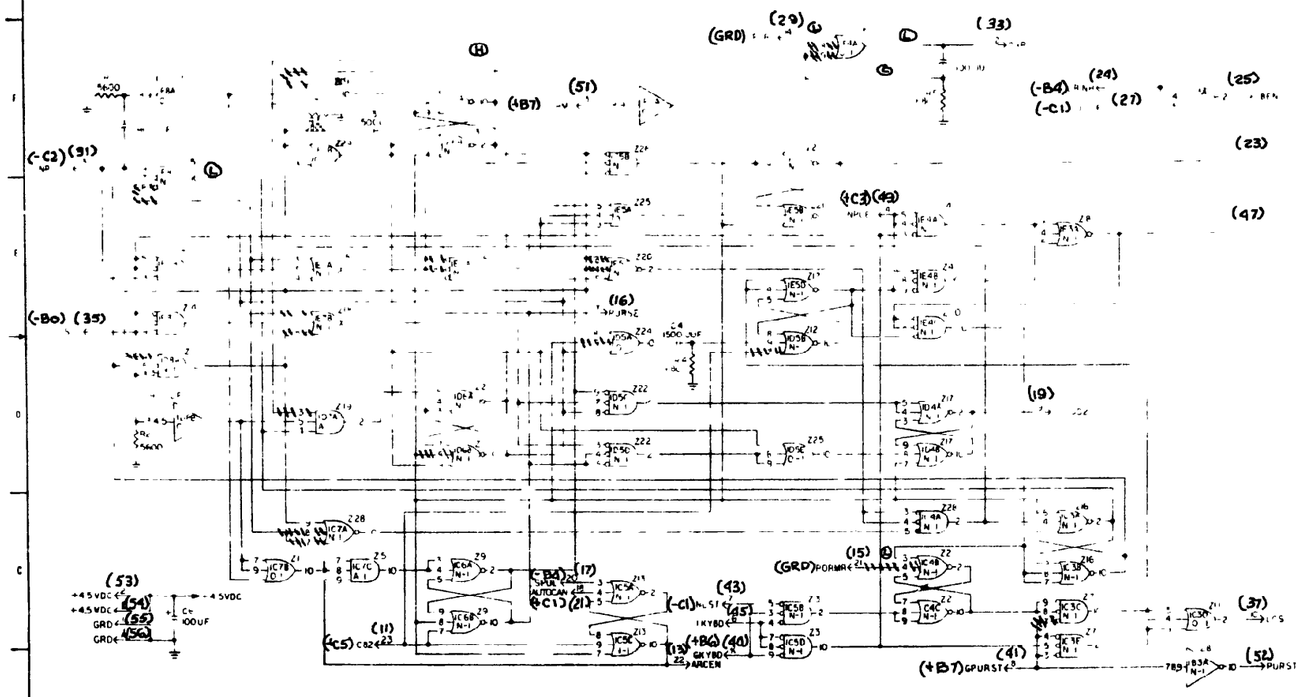
1 ICT- PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e , ARE SWITCHING DURING TEST

5 ≈≈ INDICATES UNTESTED INPUT/OUTPUT LINES



NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR TOLERANCE ARE ±5%.
   ALL RESISTOR RATINGS ARE 1/4W

POWER INPUT PINS	
	21 THRU 228
+4.5VDC	6
GRD	1

REF DES.

(-001)

SEE SEPARATE PL

GENERAL DYNAMICS
Electronics Division ROCHESTER N.Y.

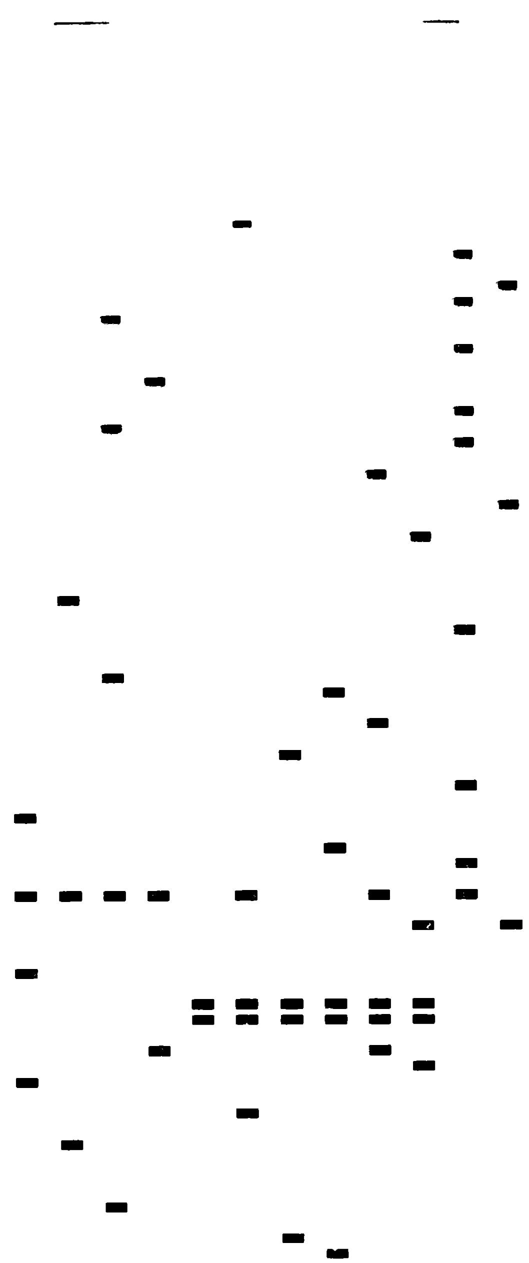
LOGIC DIAGRAM, ASSEMBLY

SIZE E | 58189 | A65008

DATE 7-6-71

P.C. Assembly A65009-001

P.C. Logic A65008 Doc. No. 23-1120-12



A65009-001 DOC. NO. 23-1120-12

"..'T AFPD. ᴵᵀ·ᴺ DATE 7-6-71"

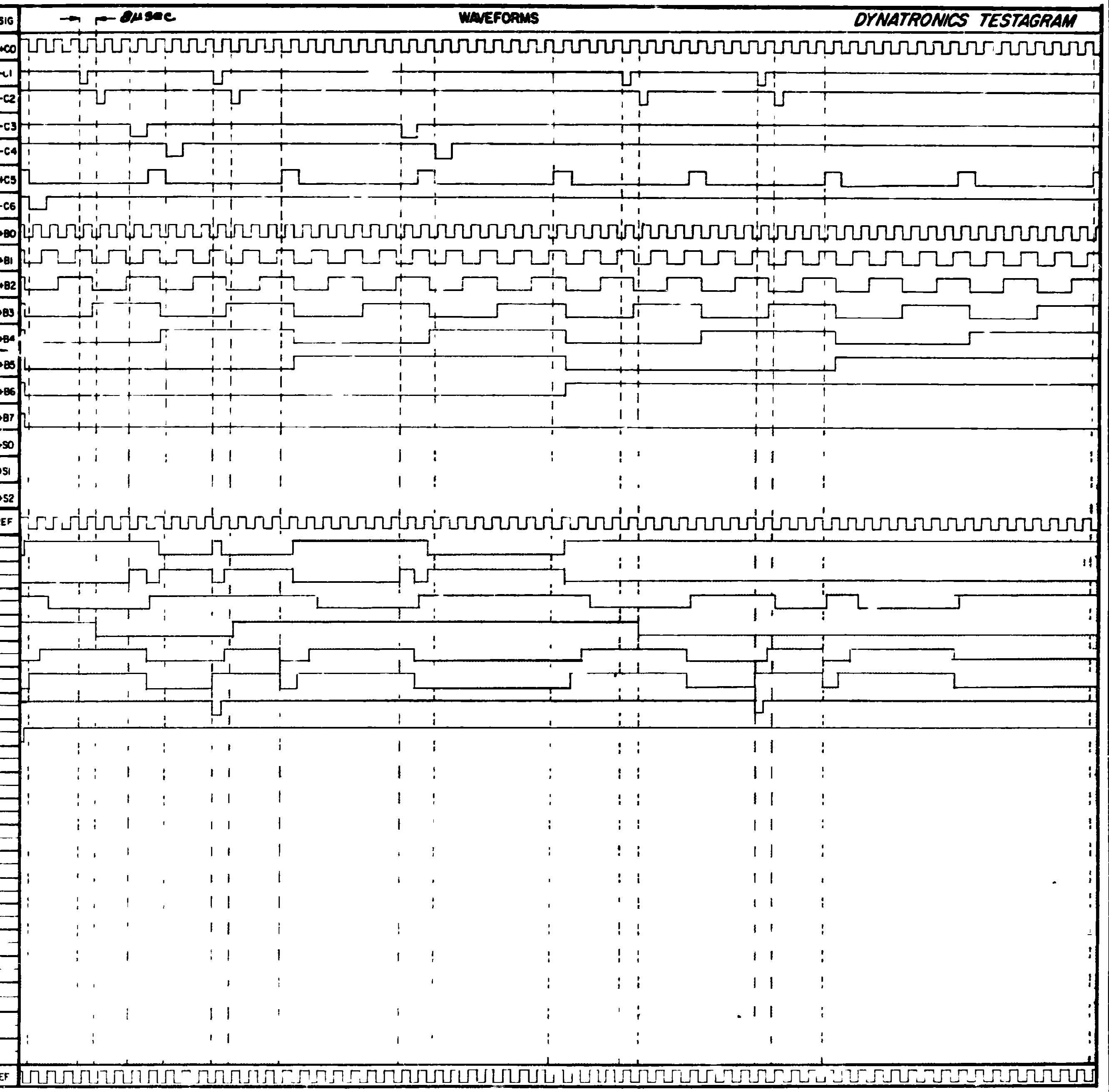
TEST PARAMETERS			
ϕVcc	4.75	SIG V	+VCC, GRD
±V	—	LOAD REF V	12=GRD 11=VCC
+V	—	CLK	2 μsec
-V	—	INT CLK	+OSC

ROW ASSIGNMENT	
10	-C2
1	C1
2	+B7
3	+B6
4	+C5
5	—
6	+C1
7	-B4
8	-B0
9	+C3

INPUT PINS	COL	SIG
	63	+C0
27, 43 21*	64	-C1
31	65	-C2
49*	66	-C3
	67	-C4
11	68	+C5
	69	-C6
35*	70	+B0
	71	+B1
	72	+B2
	73	+B3
17* 24* 40*	74	+B4
	75	+B5
45	76	+B6
41, 51	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING											
37	A	1	2	3	4	5	6	7	8	9		
	B	2	1	3	5	11	10	9	5	#		
(47)	A	1	2	3	4	5	6	7	8	9	10	11
	B	5	9	1	3	6	11	3	7	10	9	8
(19)	A	1	2	3	4	5	6	7	8	9	10	11
	B	8	10	6	8	4	6	4	5	2	4	#
(23)	A	[illegible]	2	3	4	5						
	B	8	8	4	5	#						
16	A	1	2	3	4	5	6	7				
	B	6	9	6	8	4	7	2				
13	A	1	2	3	4	5	6					
	B	3	9	3	8	1	7					
25	A	1	2									
	B	3	5									
52	A	1	2									
	B	2	5									

+C0 REF



 +B0 REF

NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

TEST LEGEND AS APPLICABLE

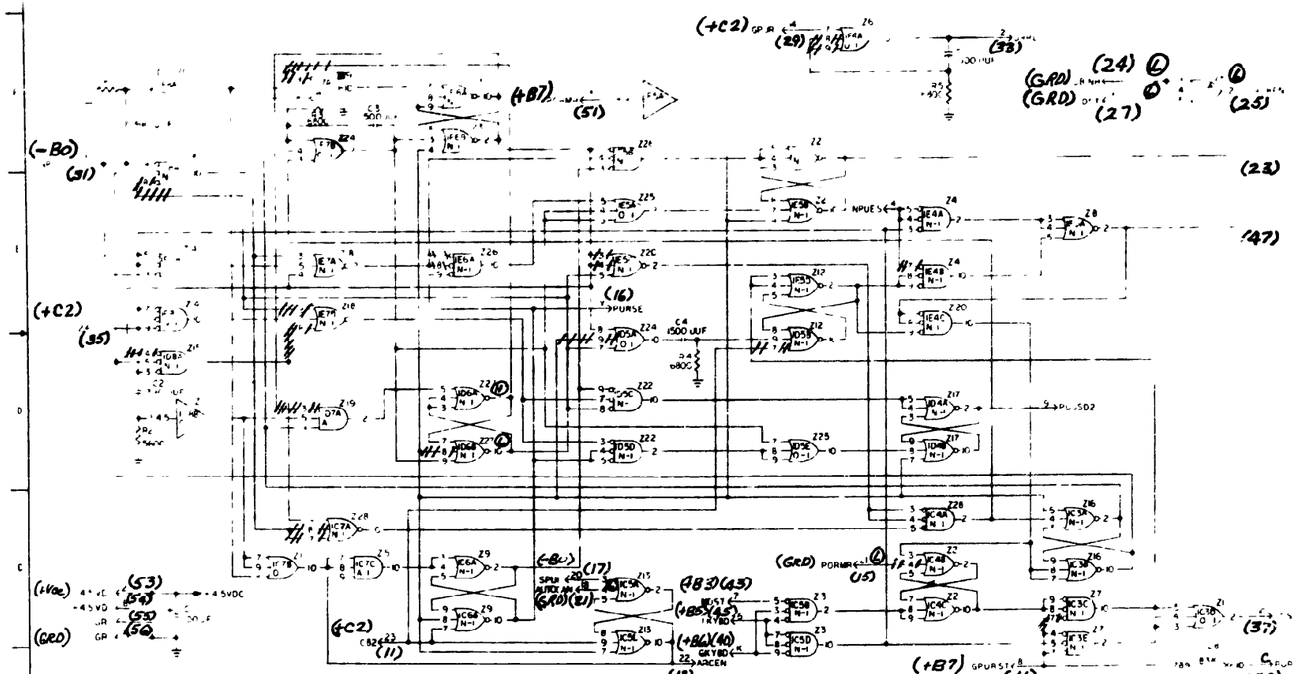
1 ICT—— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

5 ⋙ INDICATES UNTESTED INPUT/OUTPUT LINES



NOTE -

1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY SIGNATION SEE

2 UNLESS OTHERWISE SPECIFIED
- A RESISTANCE VALUES ARE IN OHMS.
- B RESISTOR TOLERANCE ARE ±5%.
- C RESISTOR RATINGS ARE 1/4W

POWER INPUT PINS	
	Z1 THRU Z28
+4.5VDC	6
GRD	1

REF WG

WIRE ASSY - A65009-001

SEE SEPARATE P1

GENERAL DYNAMICS

Electronics Division

DR-36 0394-AMC-35598E

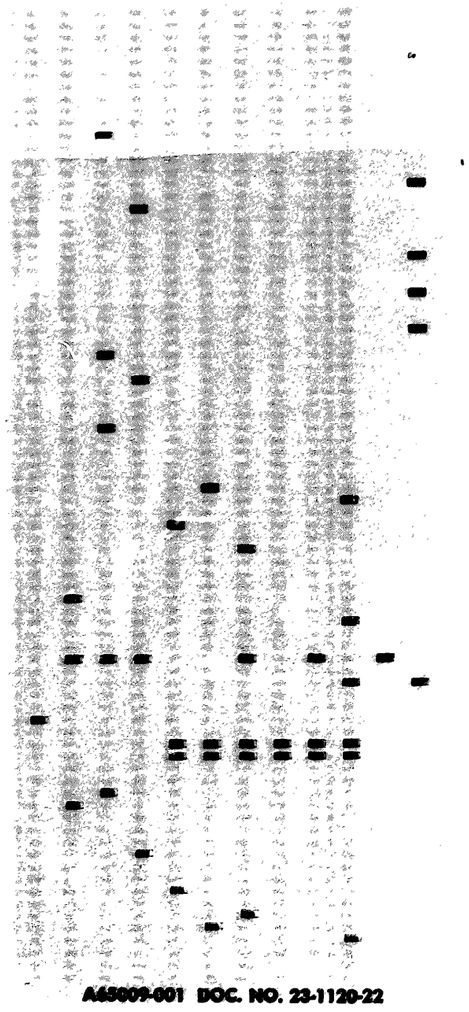
E 58189 AP 5 C 8

AUTOMATION

JN DATE 7-6-71

P.C. Assembly A65009-001

P.C. Logic A65008 Doc. No. 23-1120-22



A65009-001 DOC. NO. 23-1120-22

GOVT APPD. JW DATE 7-6-71

DYNATRONICS TESTAGRAM

TEST PARAMETERS			
Vcc	+4.75	BIG V	5=VCC, GRD
±V	—	LOAD REF V	12=GRD 11=VCC
+V	—	CLK	32µsec
-V	—	BIT CLK	+OSC

ROW ASSIGNMENT	
10	+B7
1	—
2	—
3	+B5
4	+B6
5	+B3
6	-B0
7	+C2
8	+C3
9	—

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
11,* 29,* 35*	65	-C2
49*	66	-C3
	67	-C4
	68	+C5
	69	-C6
17* 31*	70	+B0
	71	+B1
	72	+B2
43	73	+B3
	74	+B4
45	75	+B5
40	76	+B6
41 *1	77	+B7
	78	+S0
	79	+S1
	80	+S2

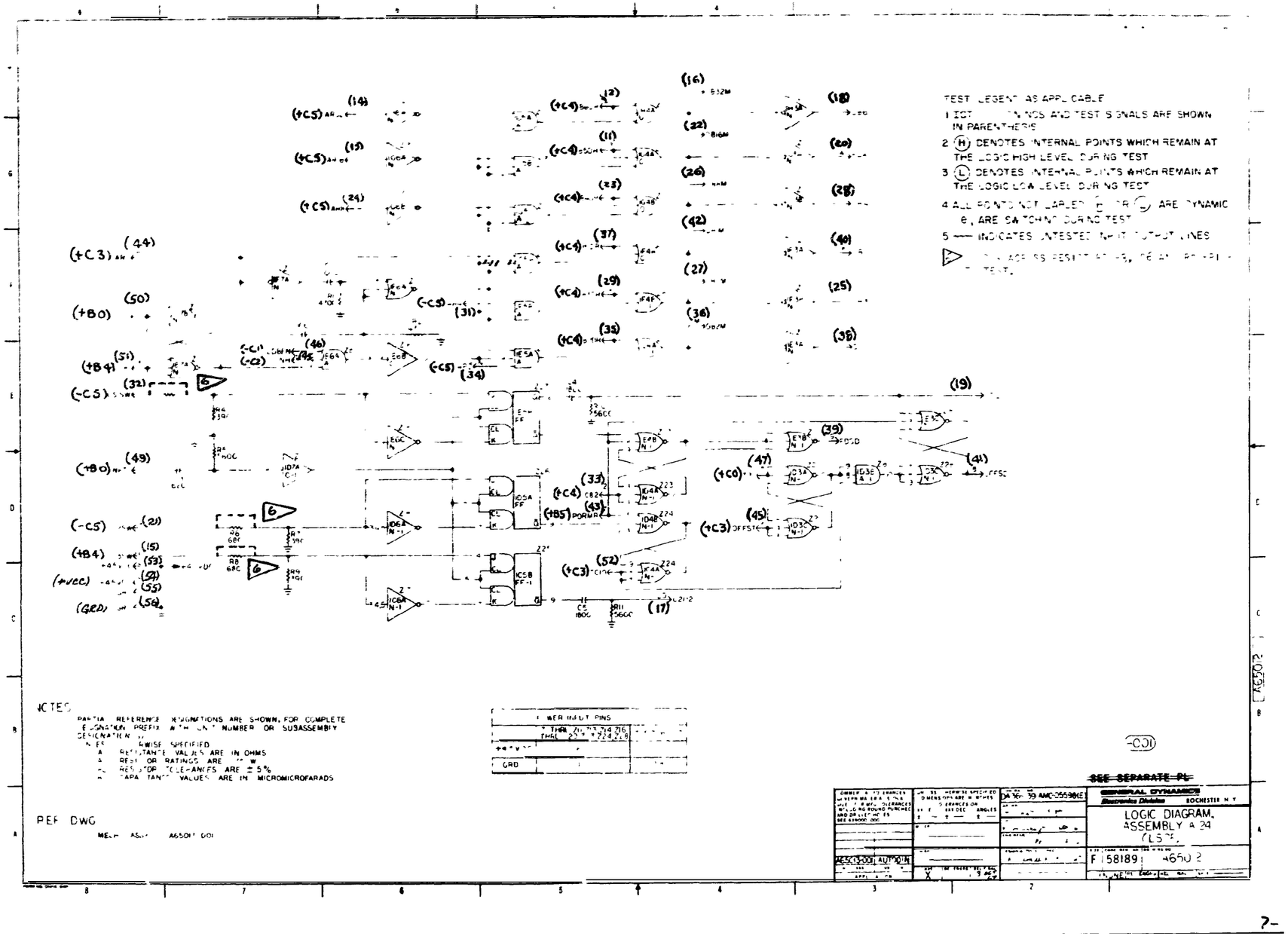
OUTPUT PINS (TEST POINTS)	SWITCH SETTING												+CO REF
㉓	A	1	2	3	4	5	6	7	8	9	10	11	
	B	4	8	3	7	[illegible]	5	9	4	8	5	#	
㊼	A	1	2	3	4	5	6	7					
	B	7	1	6	11	3	7	5					
⑲	A	1	2	3	4	5	6	7	8	9	10	11	
	B	2	9	1	8	11	6	7	5	6	5	#	
16	A	1	2	3	4								
	B	2	8	11	7								
33	A	1	2										
	B	8	10										

+ BO REF

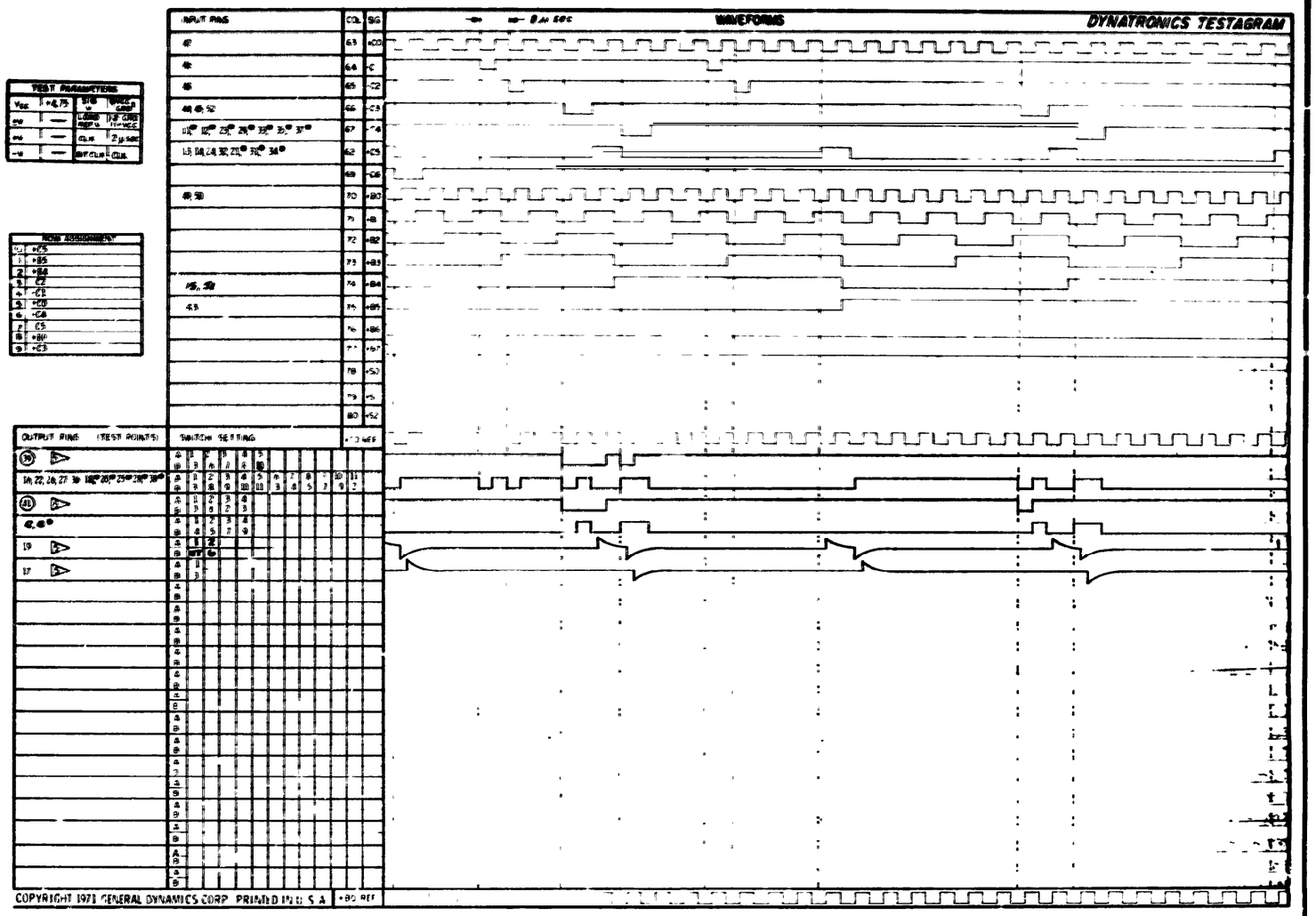
NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE BE GO/NO-GO TESTED FIRST.



P.C. Assembly A6013-001
P.C. Logic A6502 Doc. No. 23-1115-11



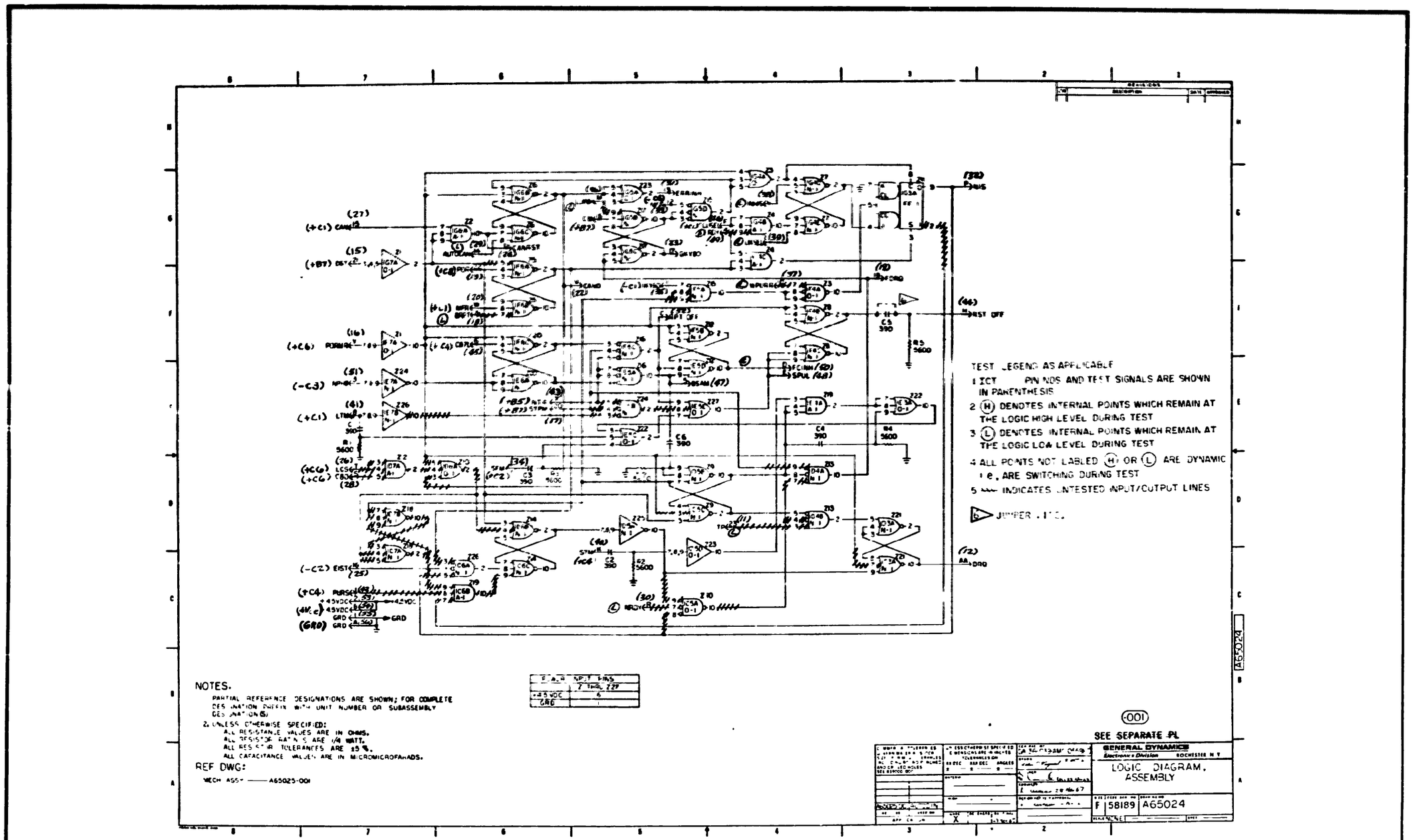
A65013-001 DOC. NO. 23-1115-11

NOTES:

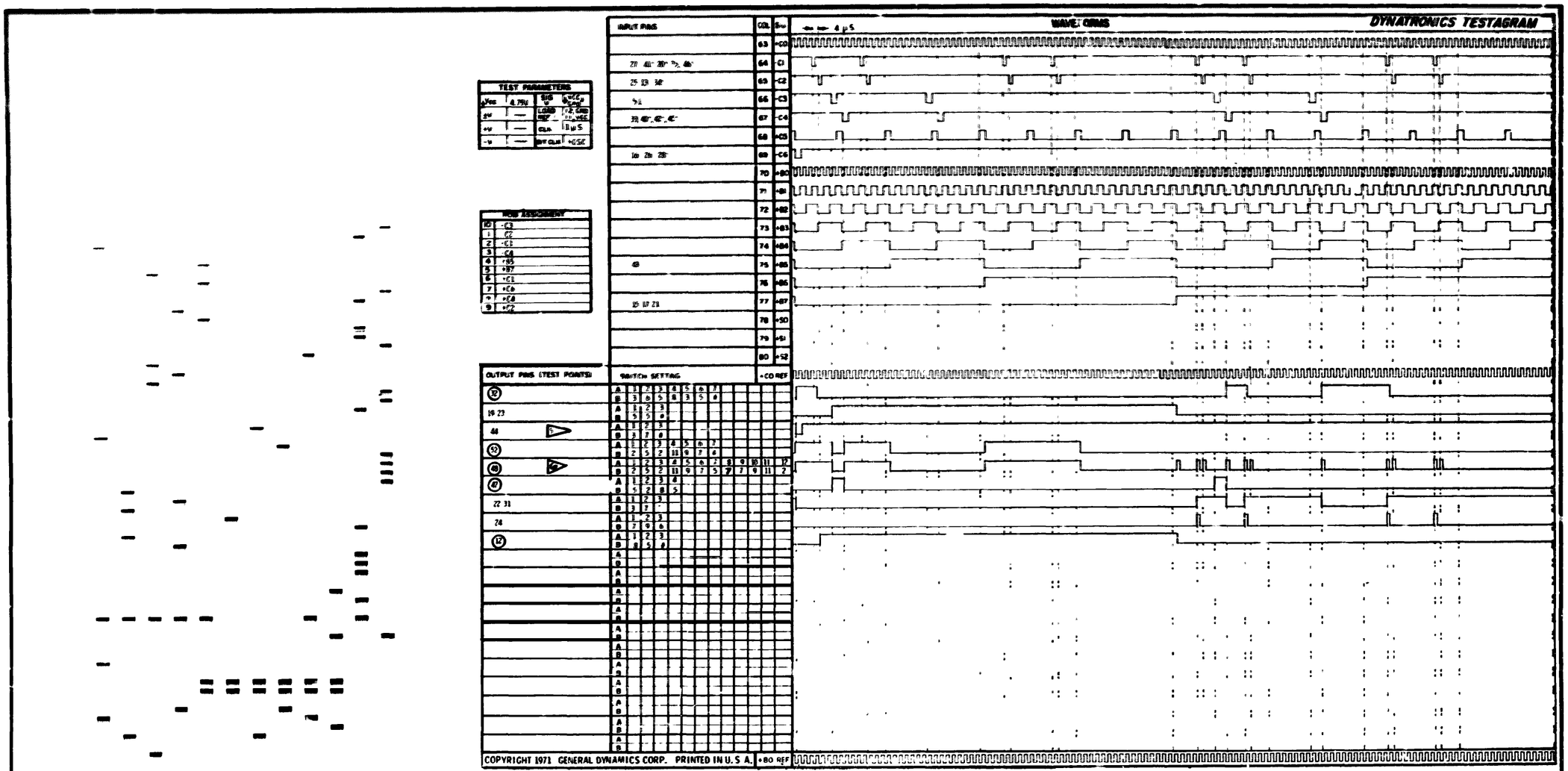
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. NT INDICATES NO TEST.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

5 SHORT OUT RESISTORS R3, R6 AND R8 PRIOR TO TEST.

7-6-71 JN


TEST LEGEND AS APPLICABLE
1 ICT PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST
5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES
JUMPER WIRE
NOTES.
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE VALUES ARE IN OHMS.
ALL RESISTOR RATINGS ARE 1/4 WATT.
ALL RESISTOR TOLERANCES ARE ±5 %.
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS.
REF DWG:
MECH ASSY —— A65025-001
(-001)
SEE SEPARATE PL
GENERAL DYNAMICS
Electronics Division ROCHESTER N.Y.
LOGIC DIAGRAM, ASSEMBLY
F 58189 A65024
A65024

7-6-71 JN



A65025-001 DOC. NO. 23-1116-12

7-6-71 JN

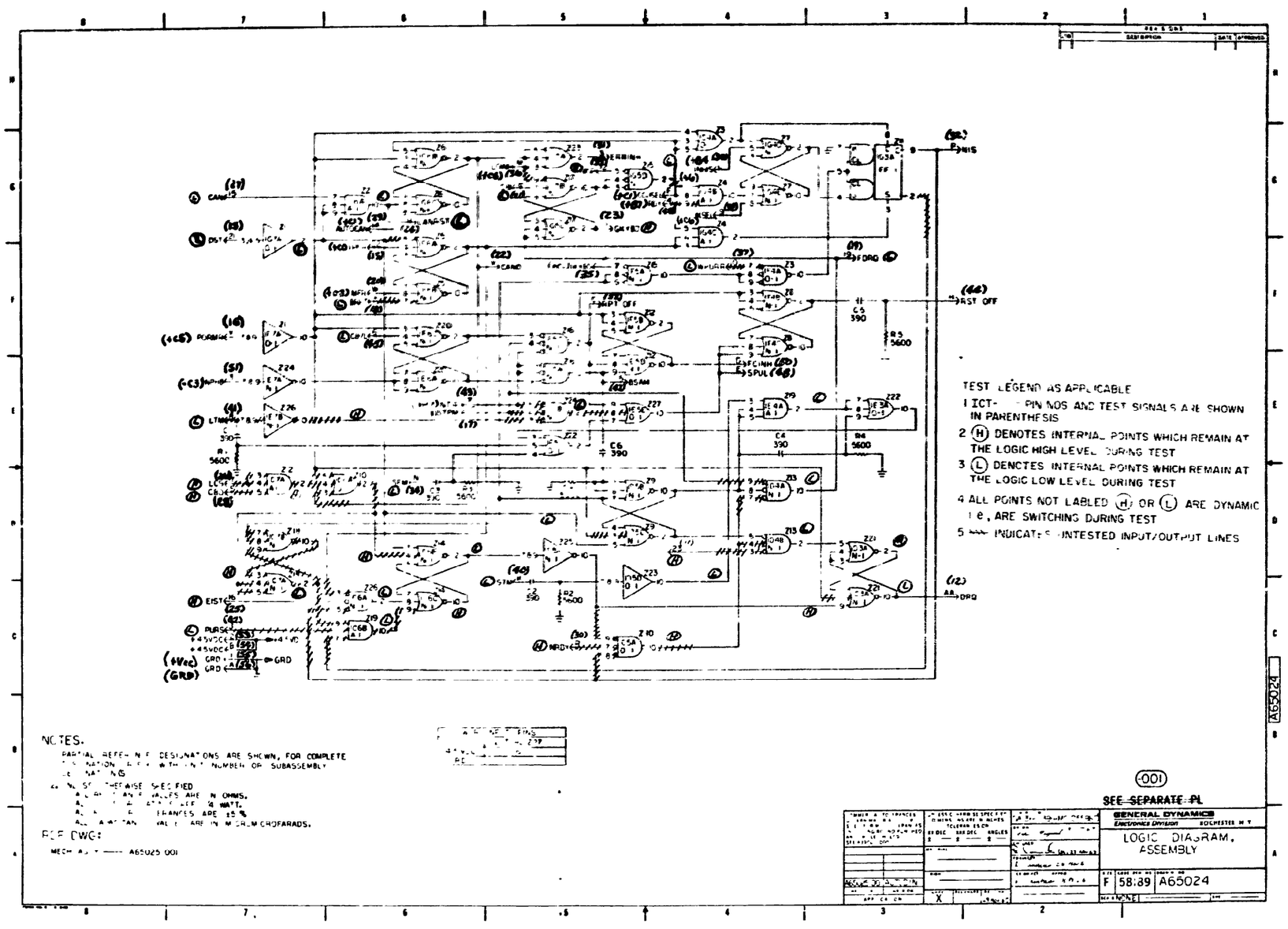
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

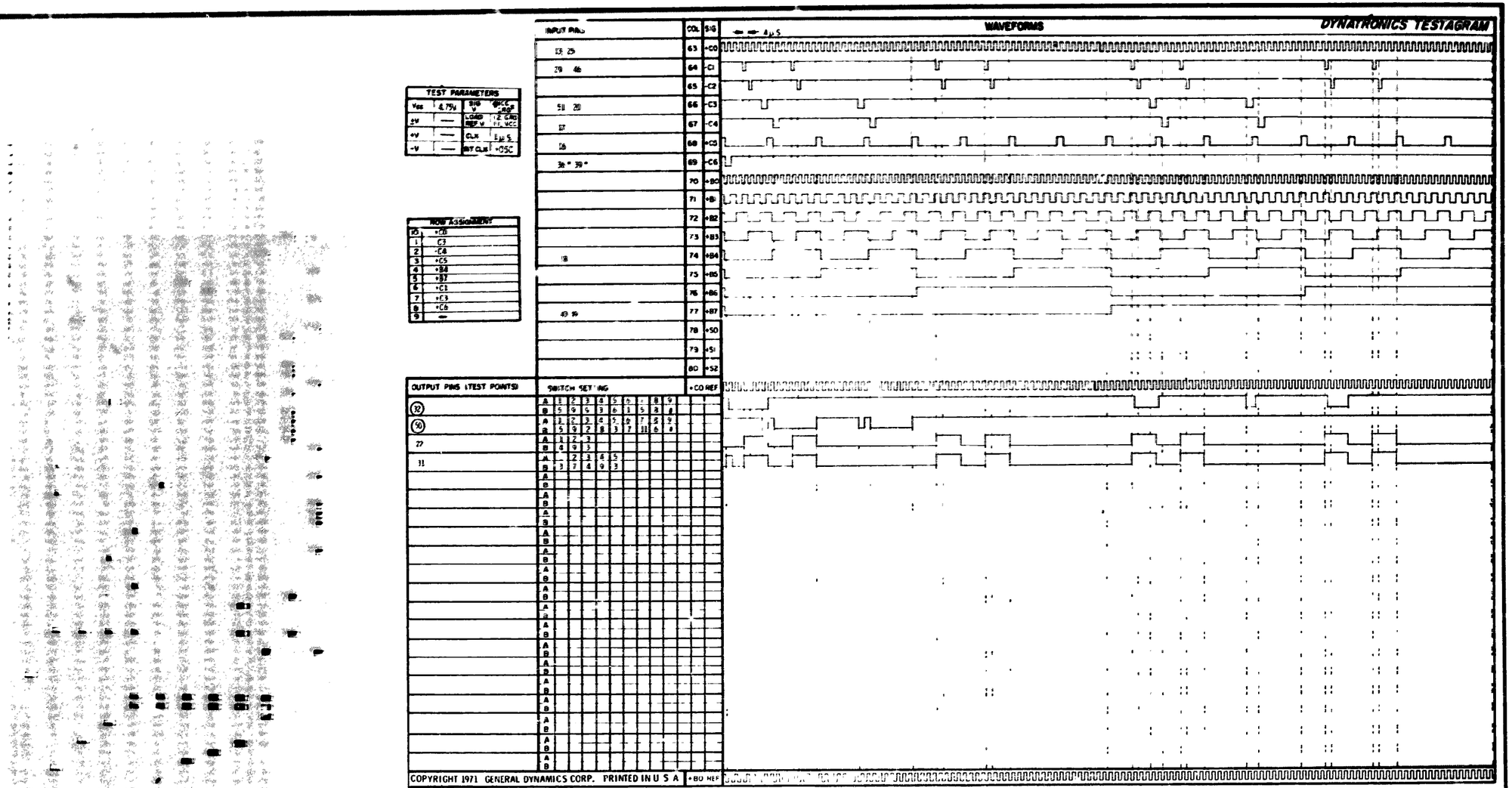
   IN ICT-103 TESTER PRESS "B" SWITCH # WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

5> INSTALL JUMPER WIRE ACROSS CAPACITOR C5 BEFORE TESTING.

6> EDGES A8, A10 AND A12 MAY INDICATE "GO" ±1 "B" SETTING FROM THAT SHOWN.


TEST LEGEND AS APPLICABLE
1 ICT- PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i e, ARE SWITCHING DURING TEST
5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES
NOTES.
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE
DESIGNATION ADD WITH ONLY NUMBER OF SUBASSEMBLY
LETTERS
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE VALUES ARE IN OHMS.
ALL RESISTORS ARE 1/4 WATT.
ALL CAPACITANCES ARE ±5%
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS.
REF DWG:
MECH ASSY —— A65025 001
(001)
SEE SEPARATE PL
GENERAL DYNAMICS
ELECTRONICS DIVISION ROCHESTER N Y
LOGIC DIAGRAM, ASSEMBLY
F 58:89 A65024
A65024

7-6-71 JN



A65025-001 DOC. NO. 23-1116-22

7-6-71 JN

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH # WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

P.C. Assembly A65025-001

P.C. Logic A65024

TEST LEGEND AS APPLICABLE

1 ICT —— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

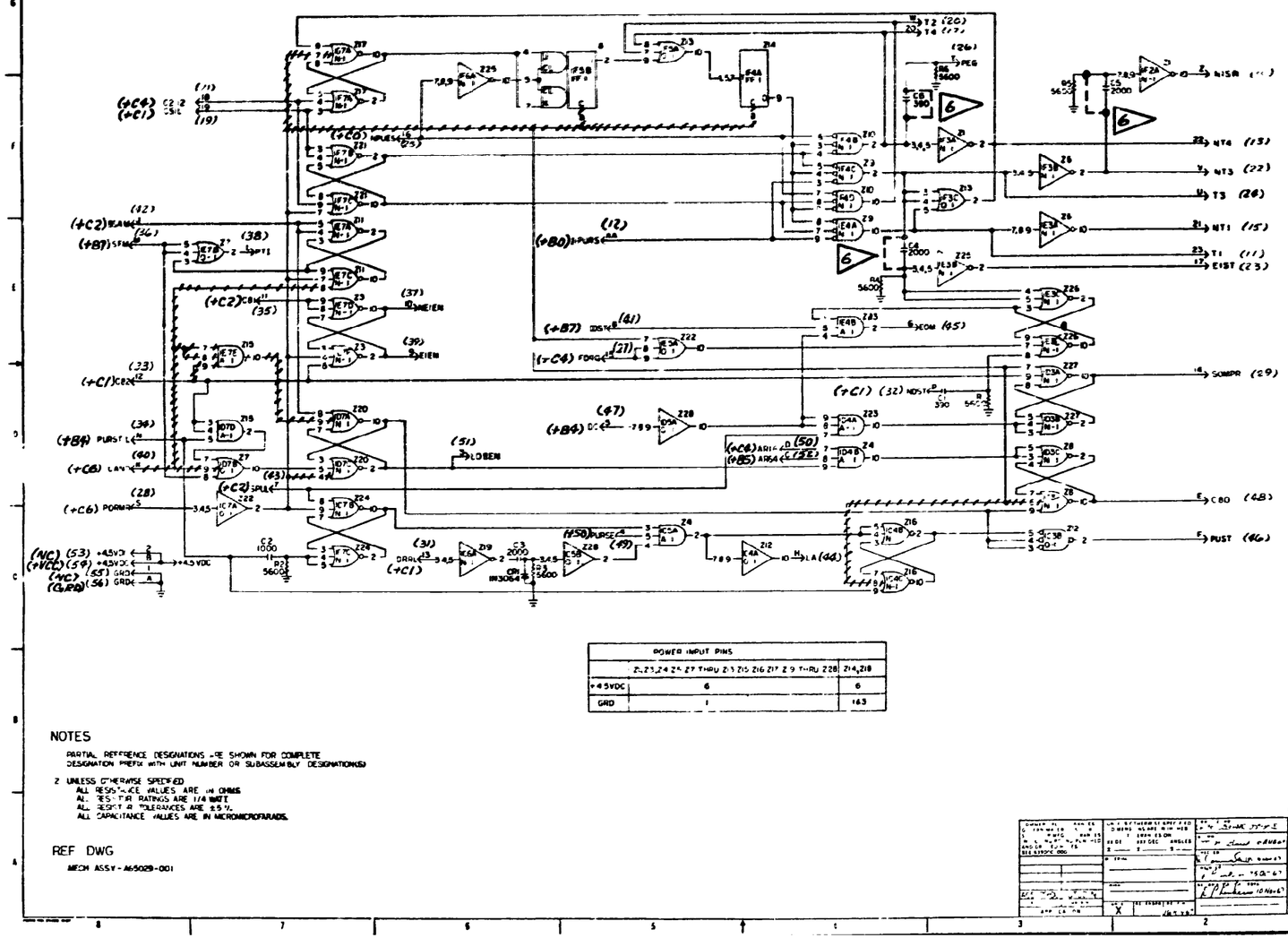
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i e, ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES

6 INSTALL JUMPER ACROSS C4,C5 AND C6 PRIOR TO TESTING CARD.



POWER INPUT PINS		
	Z1,23,24 Z4 Z7 THRU Z13 Z15 Z16 Z17 Z 9 THRU Z28	Z14,Z18
+4.5VDC	6	6
GRD	1	163

NOTES

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)

2 UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE VALUES ARE IN OHMS
ALL RESISTOR RATINGS ARE 1/4 WATT
ALL RESIST OR TOLERANCES ARE ±5%
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS.

REF DWG

MECH ASSY - A65029-001

-001

~~SEE SEPARATE PL~~

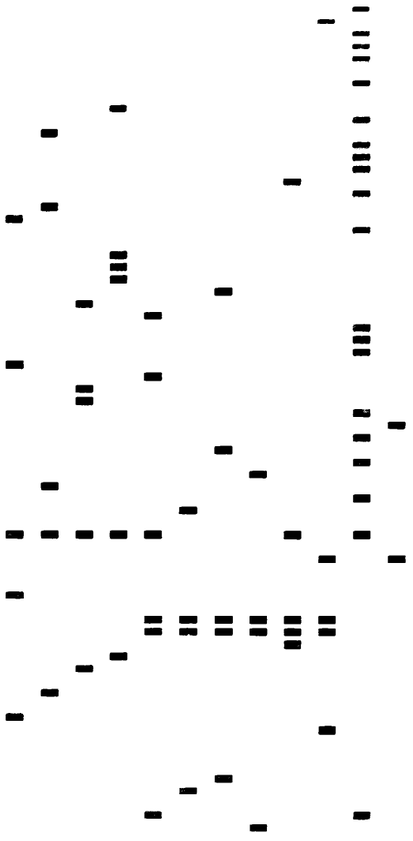
GENERAL DYNAMICS
ELECTRONICS DIVISION ROCHESTER N Y

LOGIC DIAGRAM ASSEMBLY

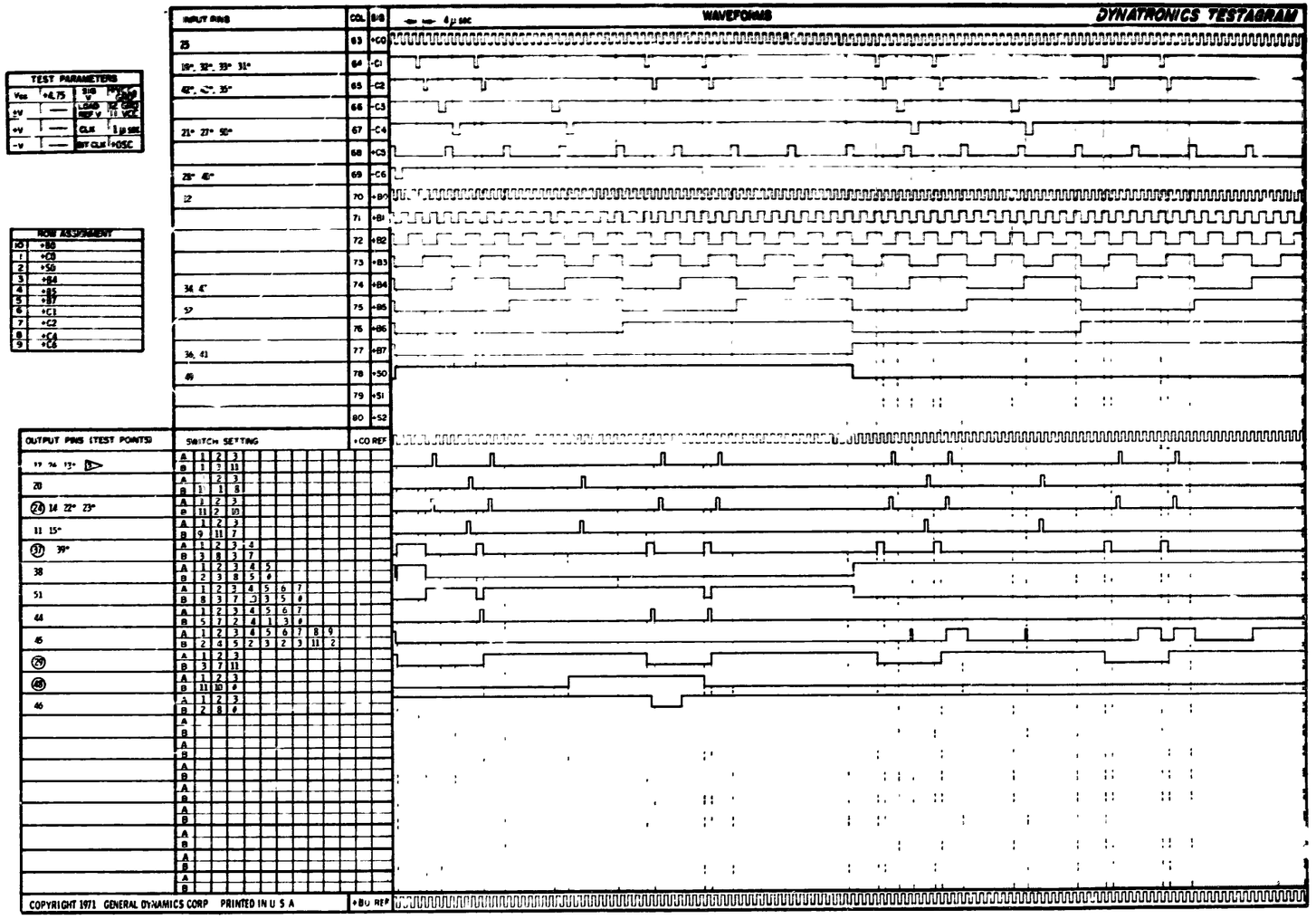
E 58189 A65028

A65028

P.C. Assembly A65029-001



A65029-001 DOC. NO. 23-1117-11

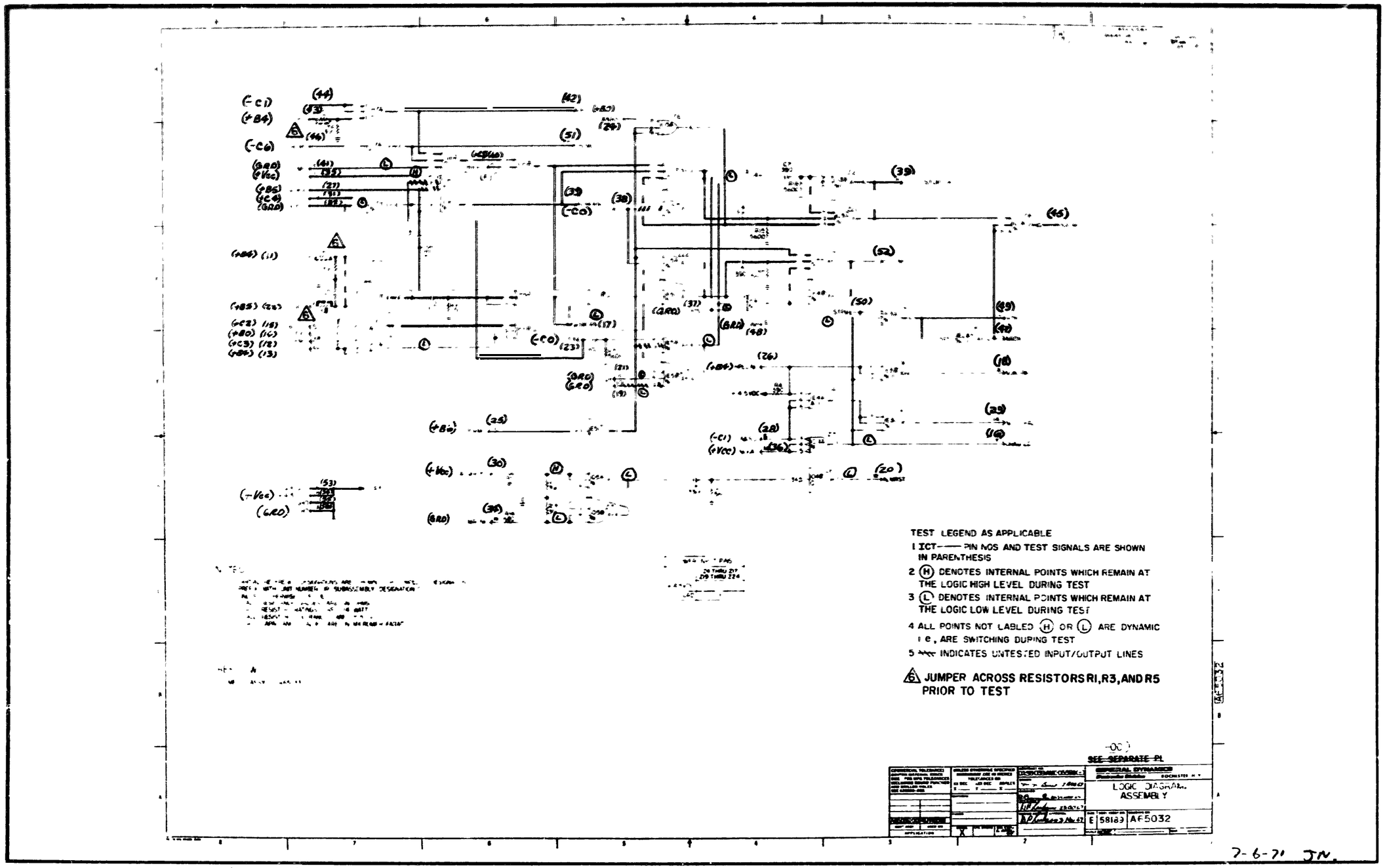


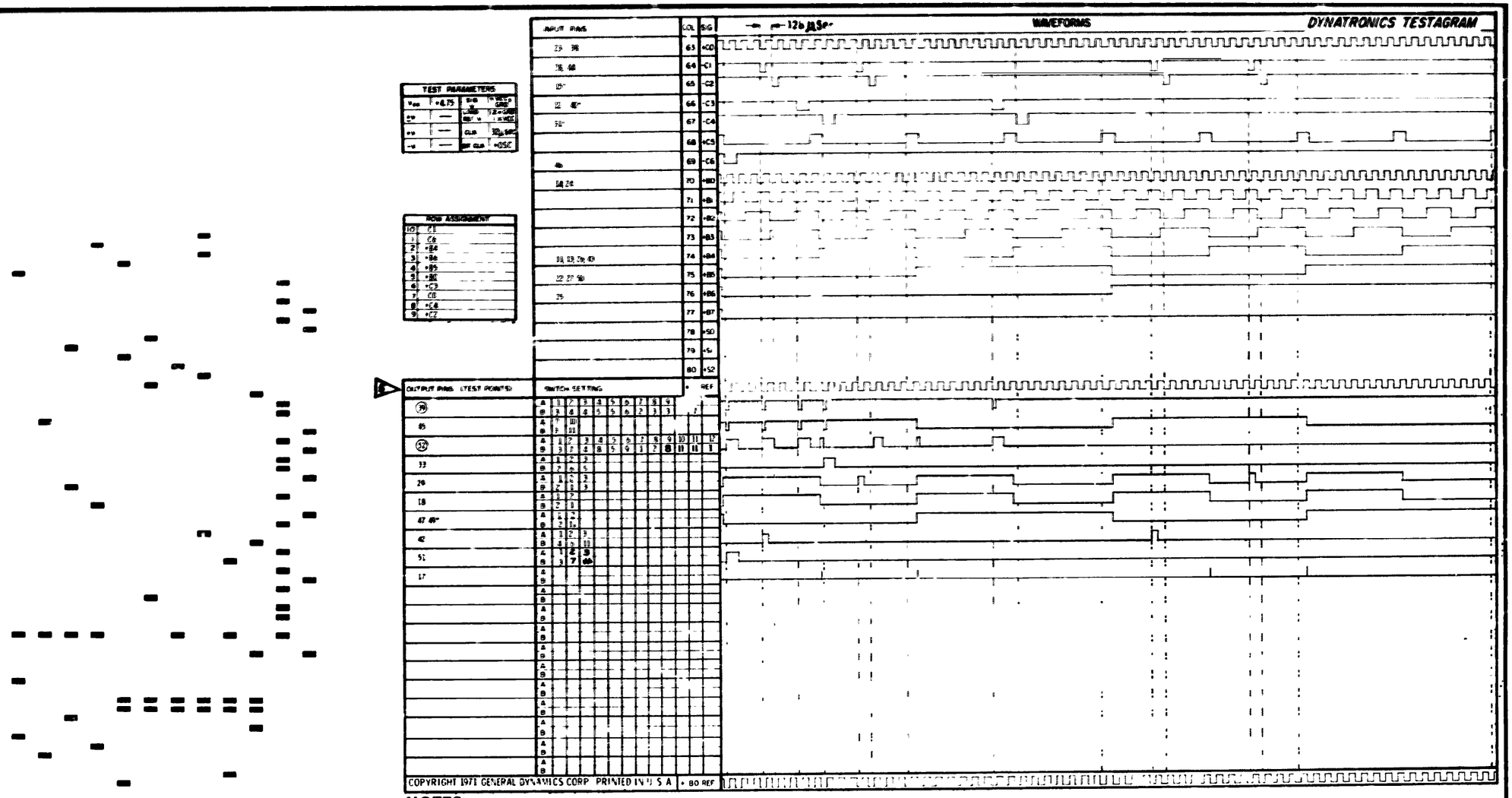
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO 4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

⑤ INSTALL JUMPERS ACROSS C4, C5 AND C6 BEFORE TESTING CARD.


TEST LEGEND AS APPLICABLE
1 ICT—— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i e, ARE SWITCHING DURING TEST
5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES
6 JUMPER ACROSS RESISTORS R1, R3, AND R5 PRIOR TO TEST
SEE SEPARATE PL
GENERAL DYNAMICS
LOGIC DIAGRAM ASSEMBLY
E 58183 AF5032
7-6-71 JN.



A65033-001 DOC. NO. 23-1118-12

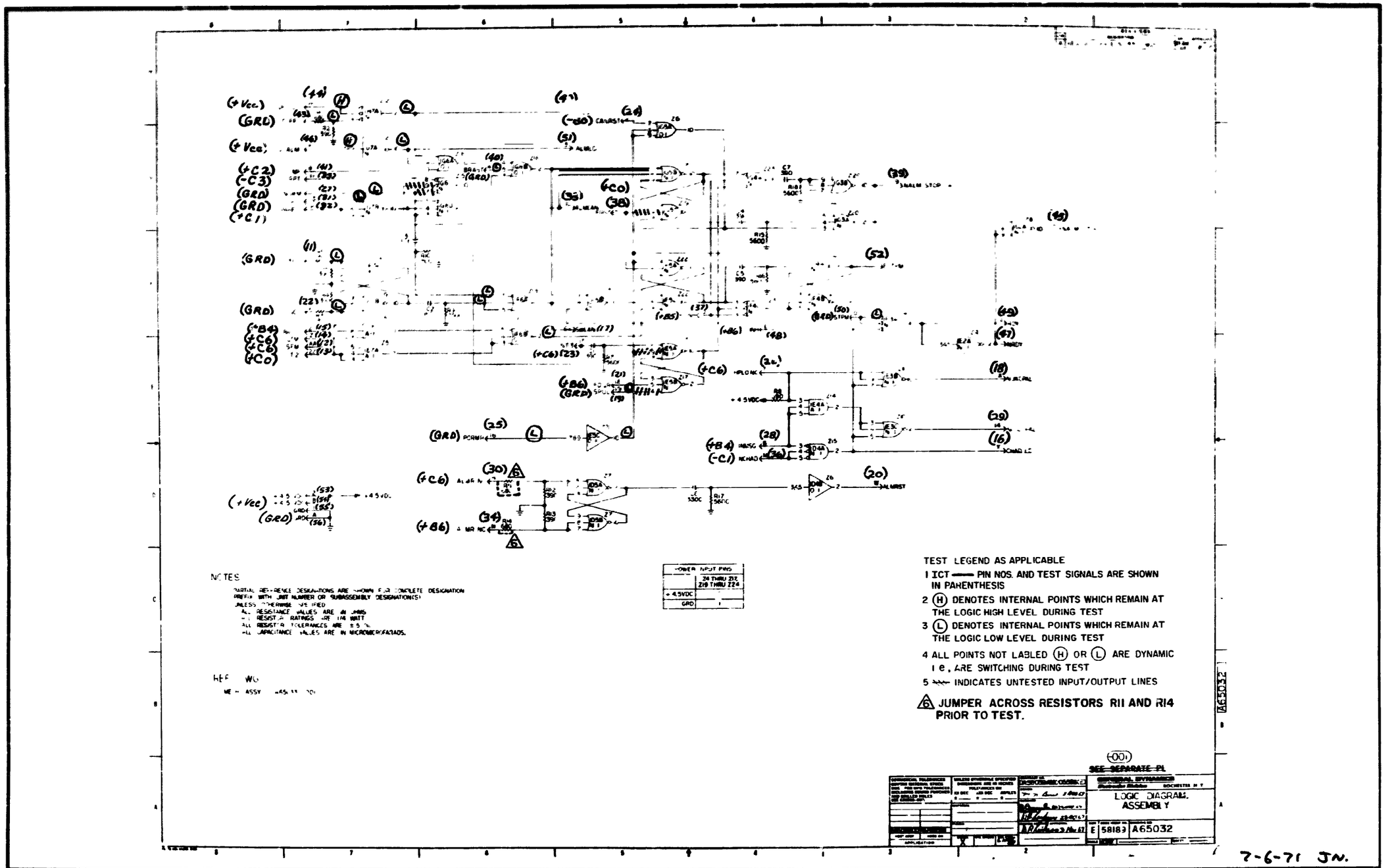
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH . "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

(5) JUMPER ACROSS RESISTORS R1, R3 AND R5 PRIOR TO TEST.

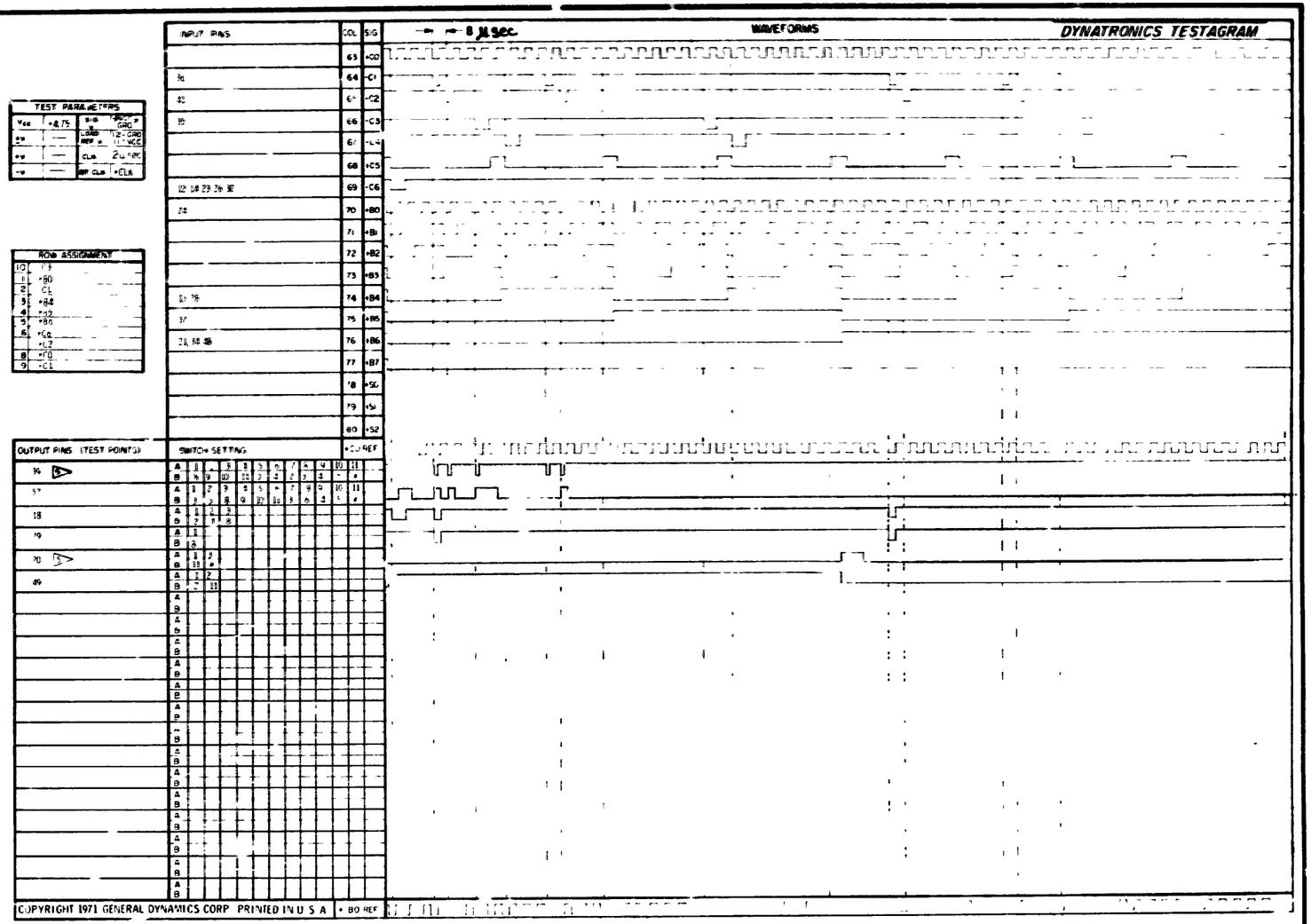
2-6-71 J.N



P.C. Assembly A65033

P.C. Logic A65032

Doc. No. 23-1118-22



A65033-001 DOC. NO. 23-1118-22

7-6-71 JN

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT, LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

(5) JUMPER ACROSS RESISTORS R11 AND R14 PRIOR TO TESTING THIS CARD.

TEST LEGEND AS APPLICABLE

ICT—— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

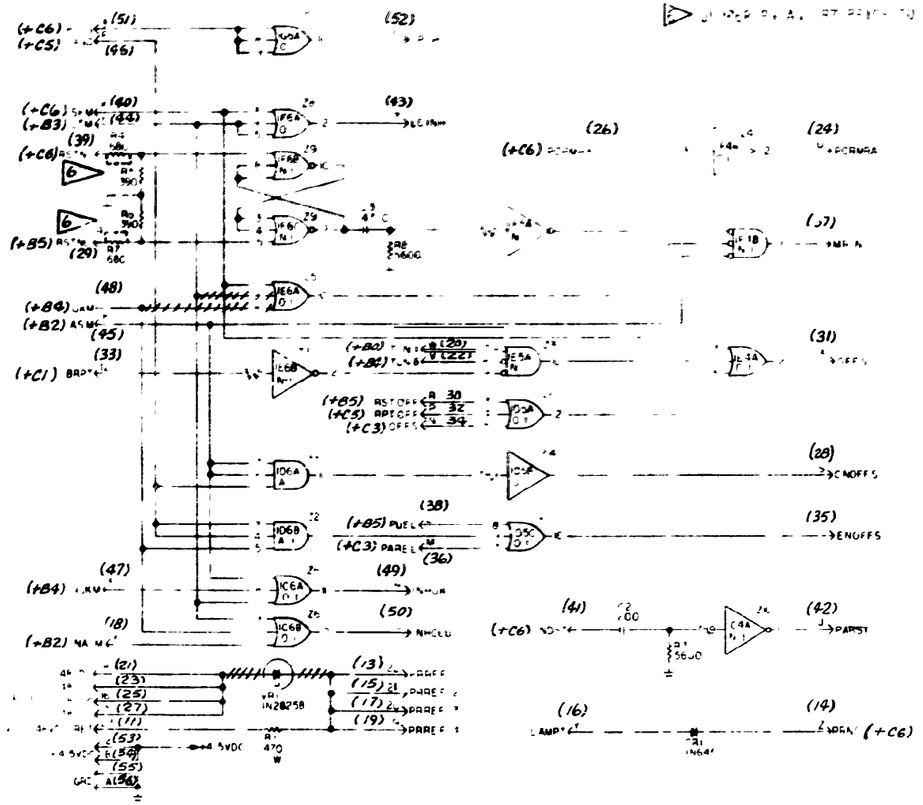
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I e, ARE SWITCHING DURING TEST

5 ≈ INDICATES UNTESTED INPUT/OUTPUT LINES

▷ [illegible] TEST.



NOTES

1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)

2 UNLESS OTHERWISE SPECIFIED

ALL RESISTANCE VALUES ARE IN OHMS

ALL RESISTOR WATTAGE RATINGS ARE 1/4 W

ALL RESISTOR TOLERANCES ARE ±5%

ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS

REF DWG

MECH ASSY [illegible]

POWER SUPPLY PINS

+4.5 V [illegible] 6

SEE SEPARATE PL

DA 36-038-AMC-05598(E)

GENERAL DYNAMICS
Electronics Division ROCHESTER, N.Y.

LOGIC DIAGRAM, ASSEMBLY

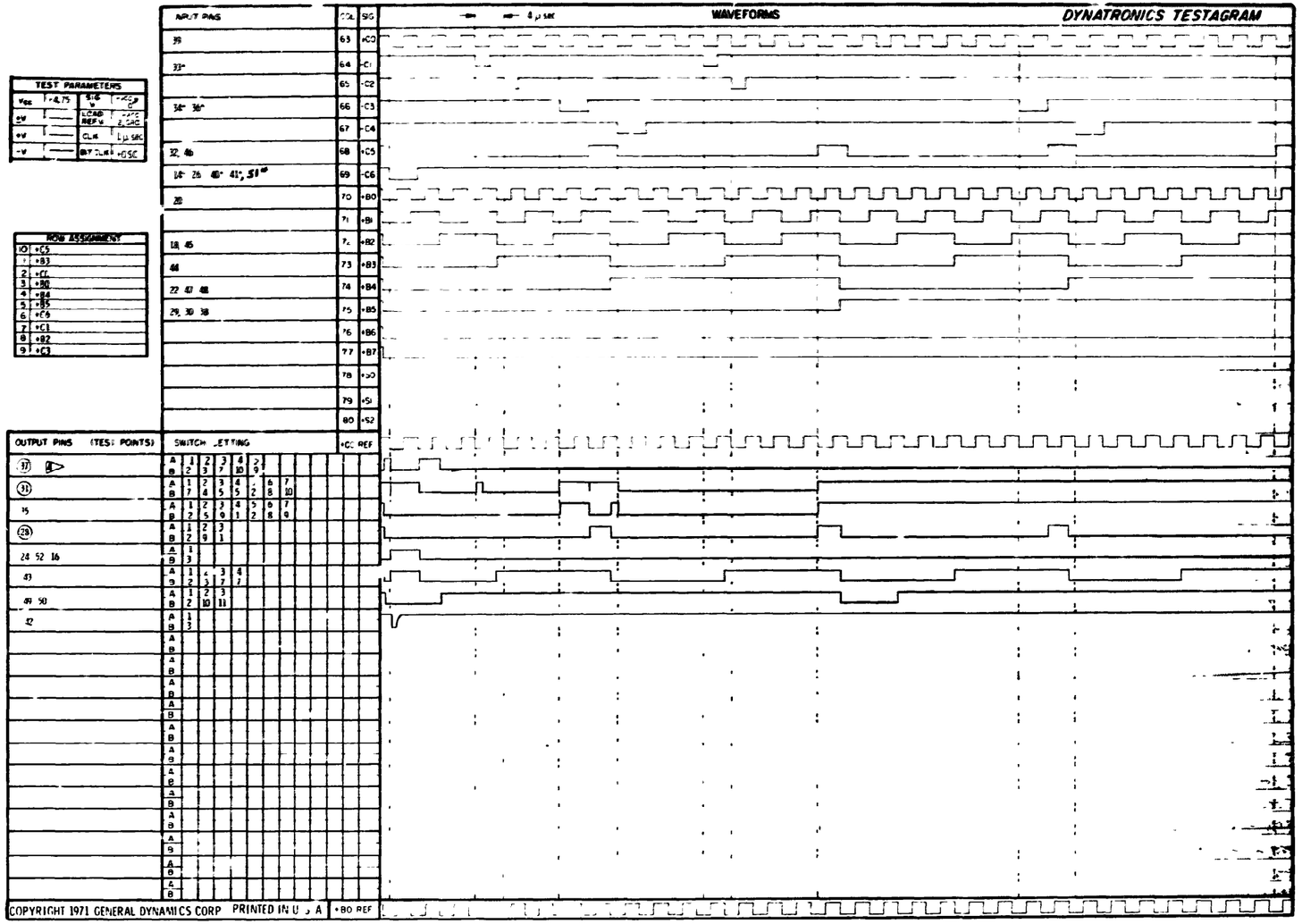
F 58189 SHEET

NONE

A65037 COR AUTODIN

7-6-71

JN



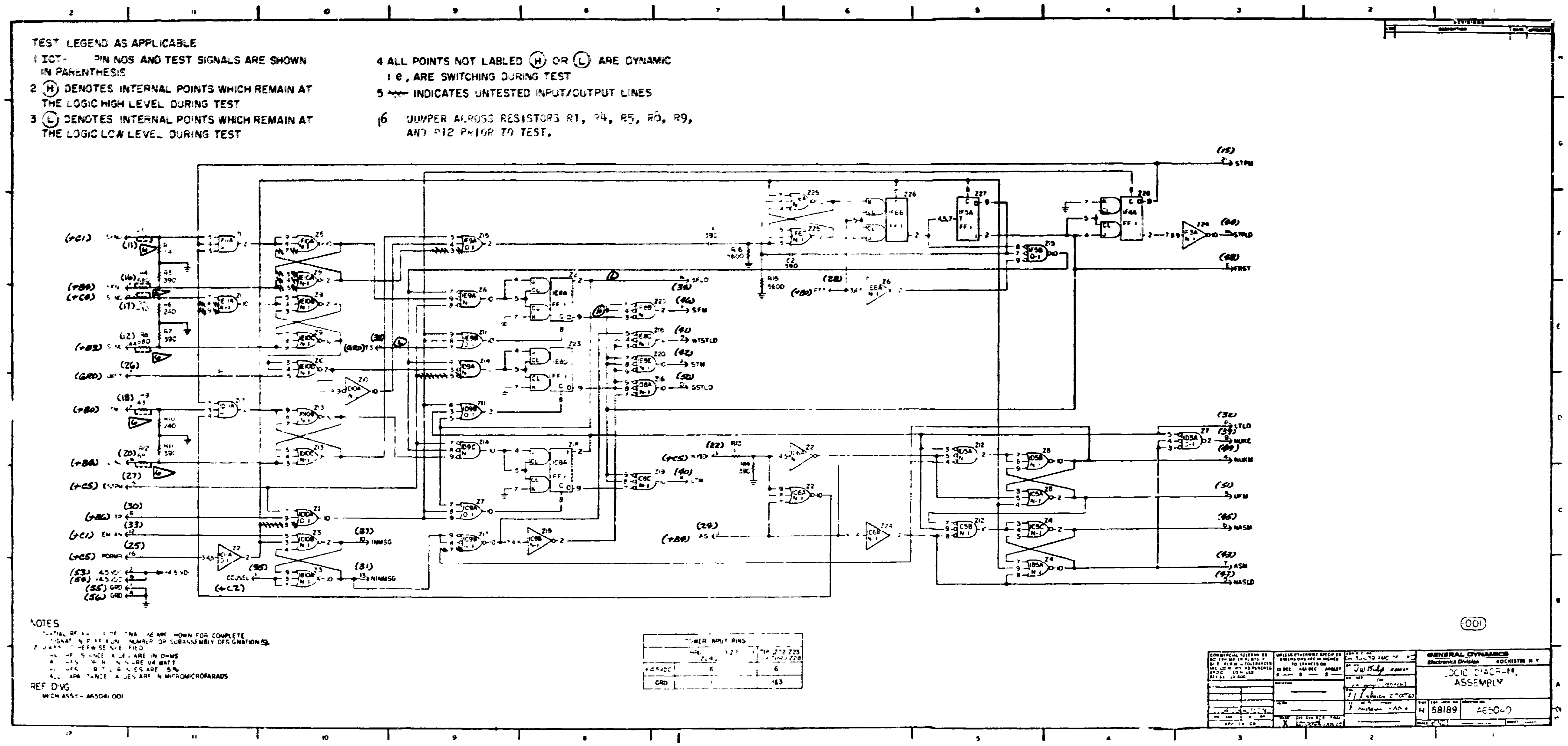
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

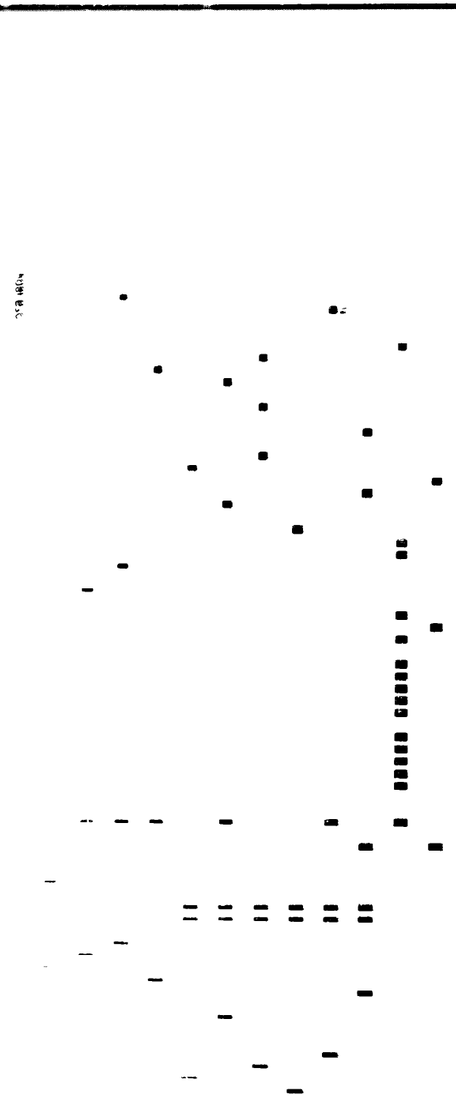
4 JUMPER ACROSS RESISTORS R4 AND R7 PRIOR TO TEST.

A65037-001 DOC. NO. 23-2111-11

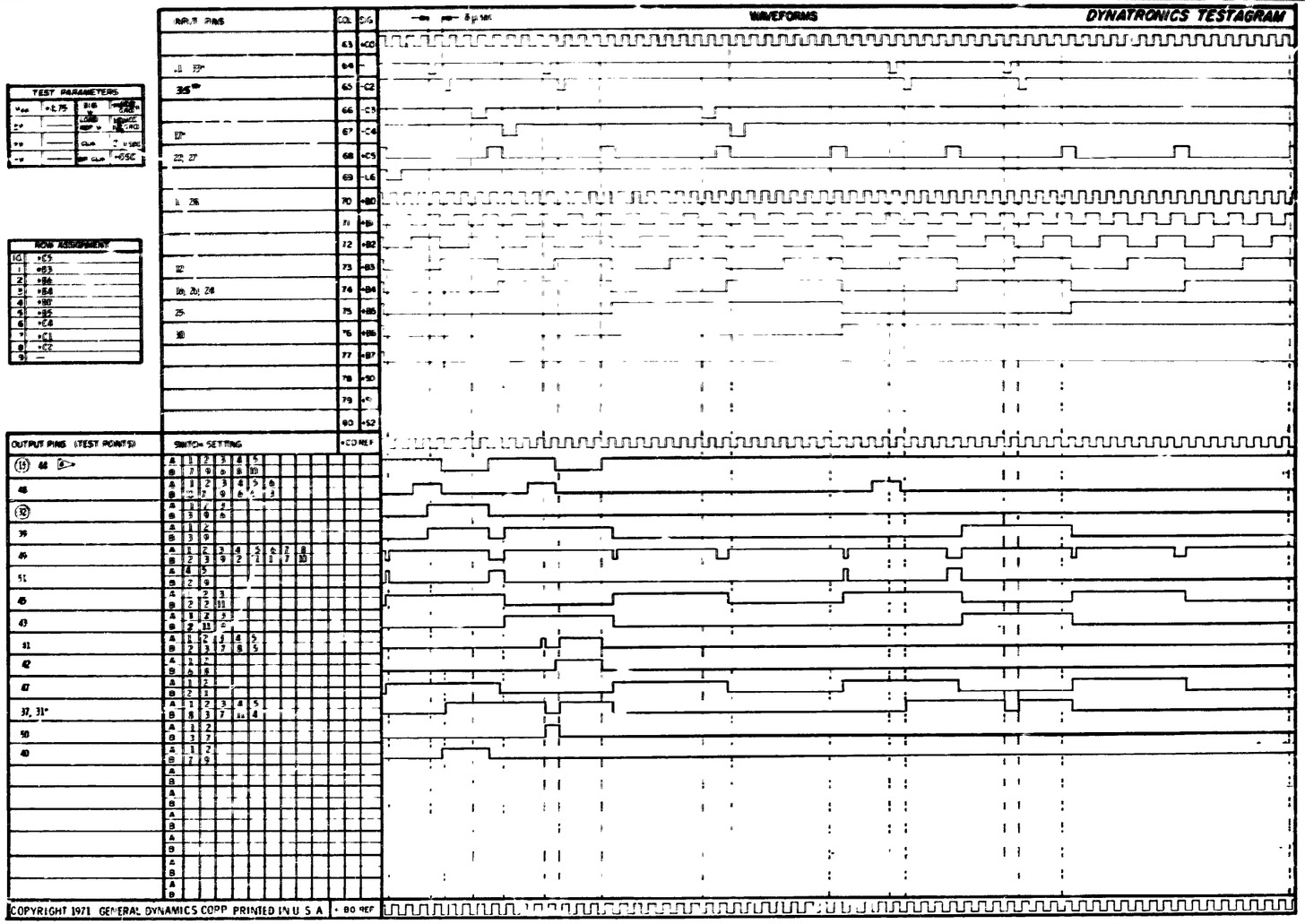
GOVT APPD. JN DATE 7-6-71


TEST LEGEND AS APPLICABLE
1 ICT- PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST
5 INDICATES UNTESTED INPUT/OUTPUT LINES
6 JUMPER ACROSS RESISTORS R1, R4, R5, R8, R9, AND R12 PRIOR TO TEST.
NOTES
REF DWG
GENERAL DYNAMICS
Electronics Division
ROCHESTER N Y
LOGIC DIAGRAM, ASSEMBLY
58189
A65040
001

JN 7-6-71



A65041-001 DOC. NO. 23-2112-12



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

4 JUMPER ACROSS RESISTORS R1, R4, R5, R8, R9, AND R12 PRIOR TO TEST.

GOVT APPD. JN DATE 7-6-71

TEST LEGEND AS APPLICABLE

1 ICT— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

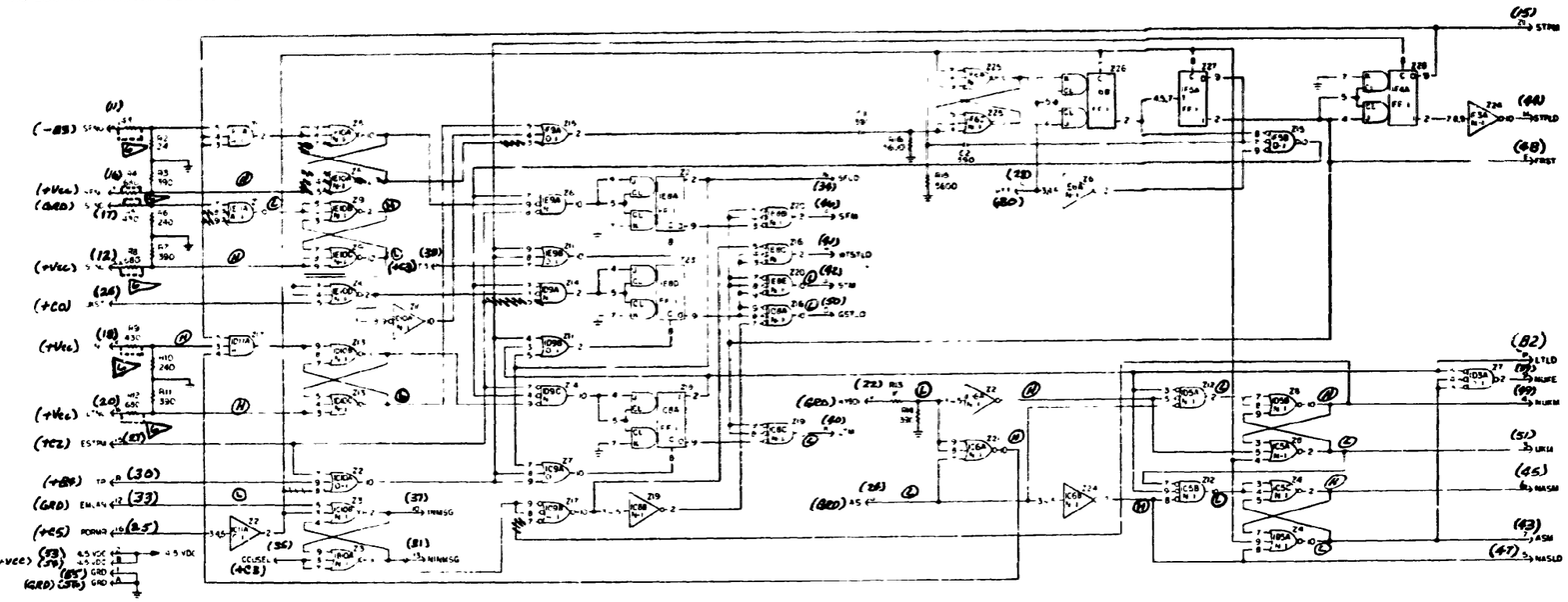
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST

5 ⚡ INDICATES UNTESTED INPUT/OUTPUT LINES

6 JUMPER ACROSS RESISTORS R1, R4, R5, R8, R9, AND R12 PRIOR TO TEST.



P.C. Assembly A65041

P.C. Logic A65040

A65041-001 DOC. NO. 23-2112-22

GOVT APPD. JN DATE 7-6-71

TEST PARAMETERS			
V_{CC}	+4.75	SIG V	+CC
0V		LOAD	
0V		CLR	1 μ SEC
-V		SYS CLK	÷OSC

ROW ASSIGNMENT	
10	+VCC
1	+B0
2	+B4
3	+C3
4	LB
5	—
6	—
7	+C3
8	+C2
9	B3

INPUT PINS	TOL	SIG
26	63	+C0
	64	+C1
	65	C2
35 38	66	C3
	67	+C4
25	68	+C5
	69	-C6
28	70	+B0
	71	+B1
	72	+B2
22	73	+B3
30	74	+B4
	75	+B5
	76	+B6
	77	-B7
	78	+S0
	79	+S
	80	+S2

OUTPUT PINS (TEST POINTS) SWITCH SET +CO OFF

WAVEFORMS — 4 μ SEC

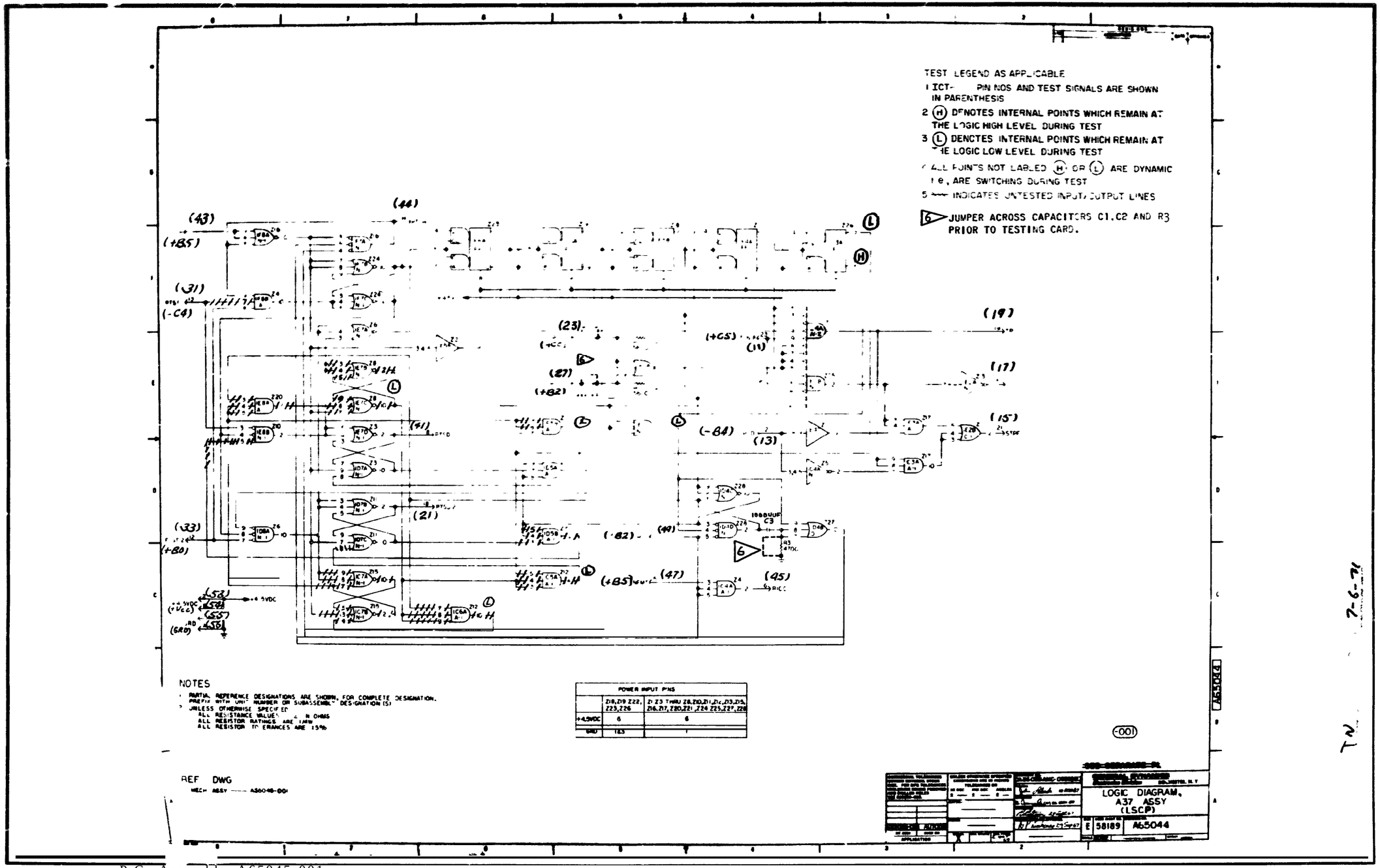
DYNATRONICS TESTAGRAM

 +B0 REF

NOTES:

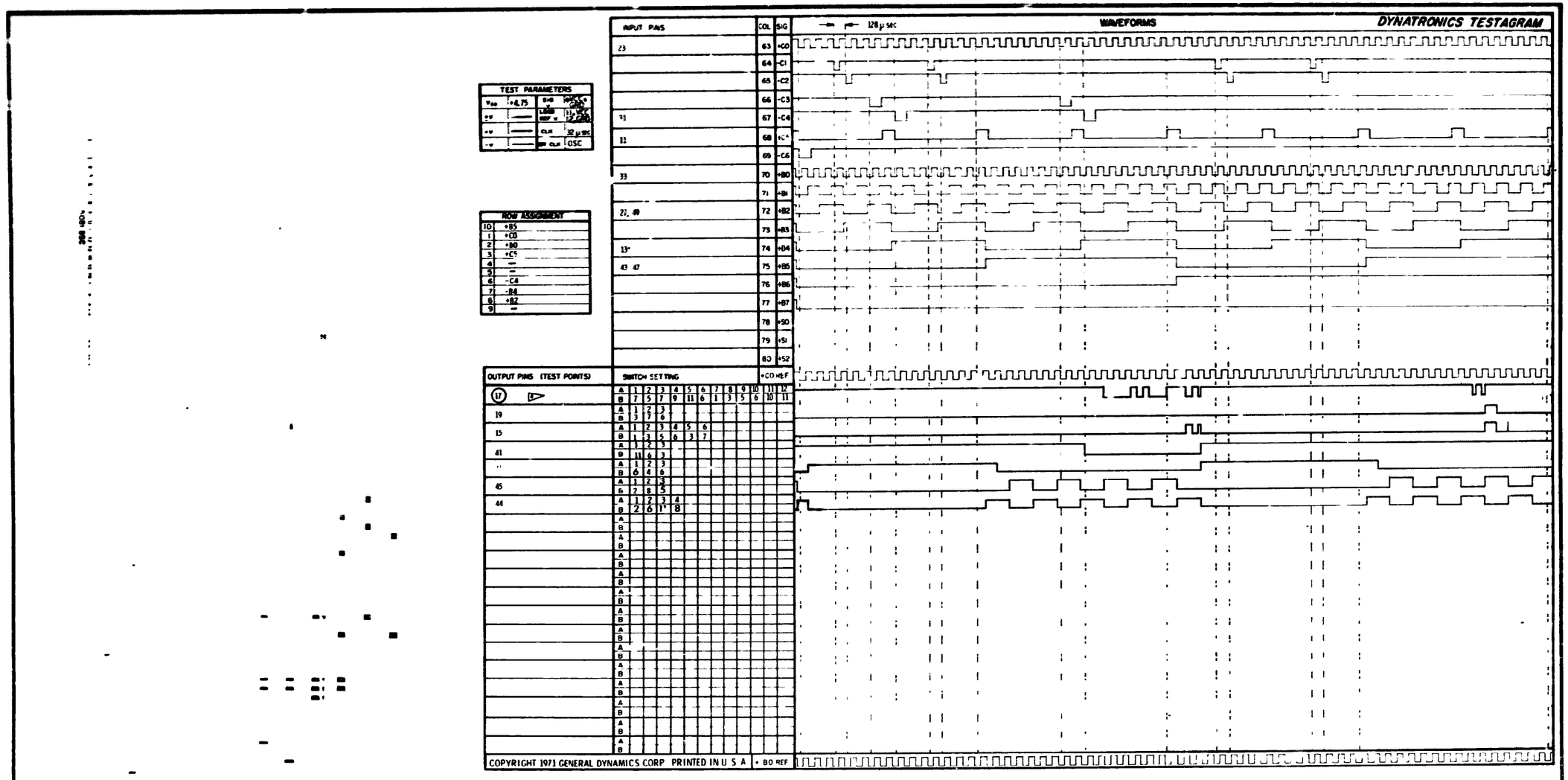
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EX1) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

4 JUMPER ACROSS RESISTORS R1, R4, R5, R8, R9 AND R12 PRIOR TO TEST.



P.C. Assembly A65045-001

P.C. Logic A65044



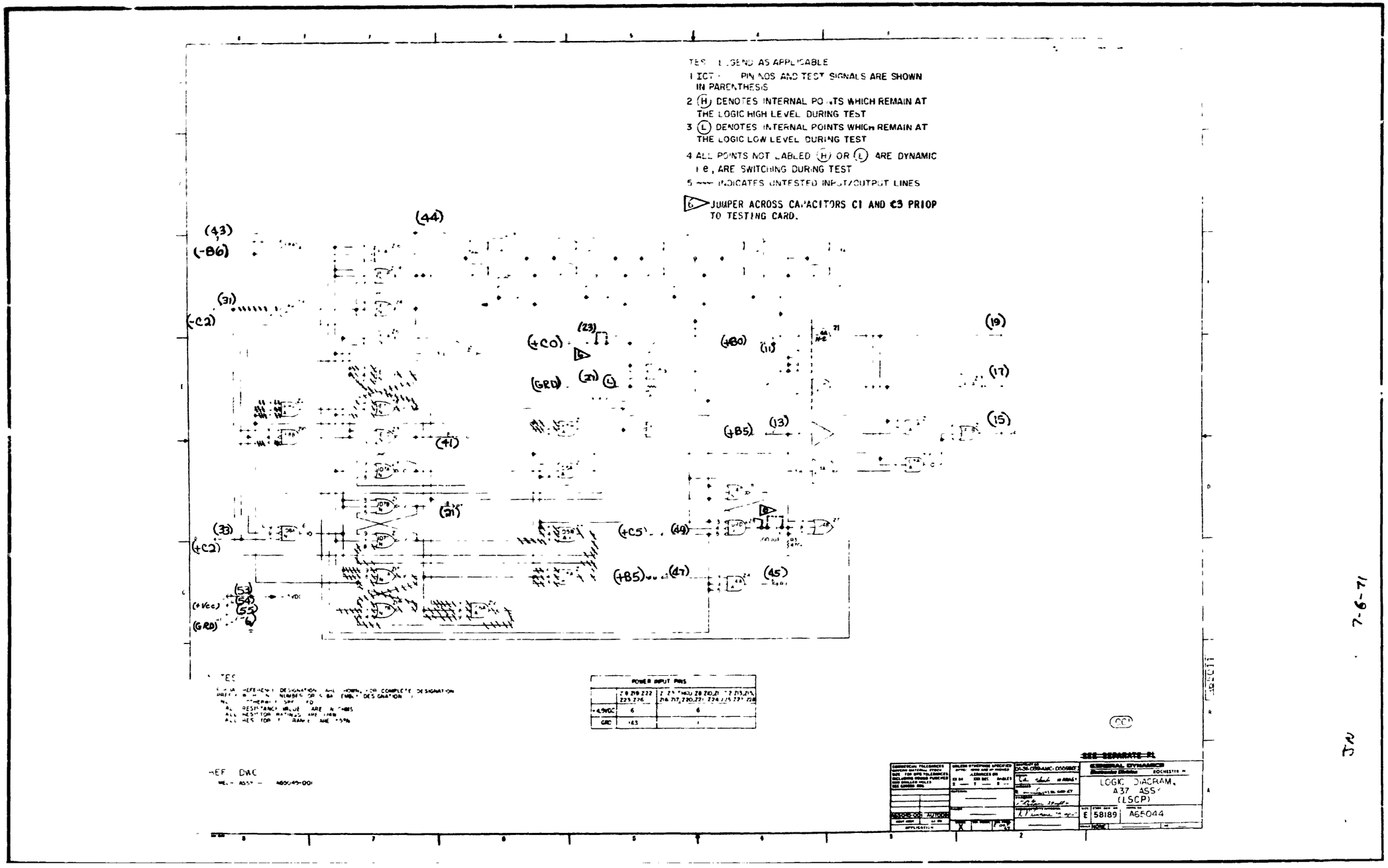
A65045-001 DOC. NO. 23-2113-12

GOVT APPD. JN DATE 7-6-71

NOTES:

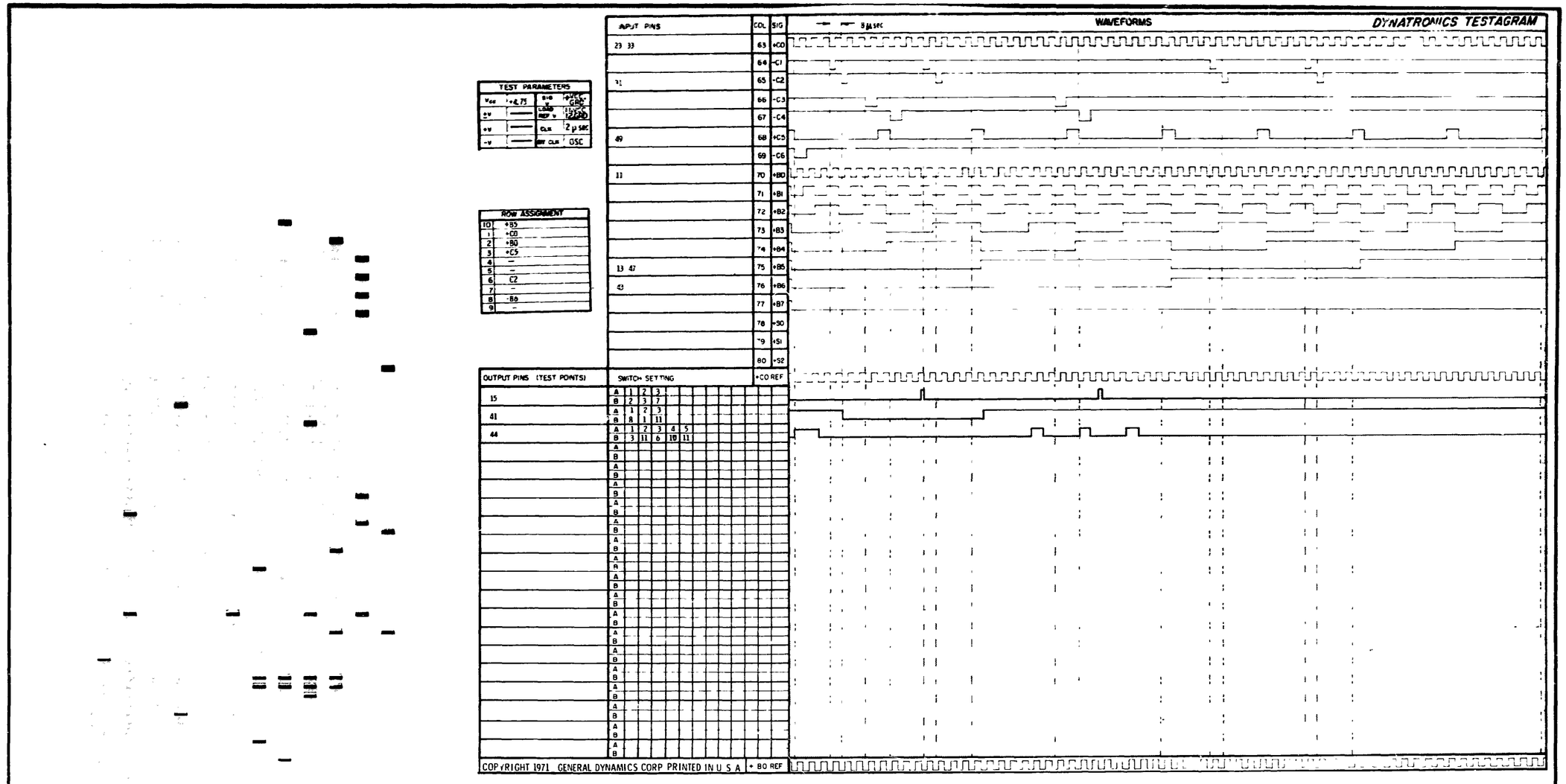
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

4 JUMPER ACROSS C1, C2 AND R3 PRIOR TO TEST.



P.C. Assembly A65045-001

P.C. Logic A65044

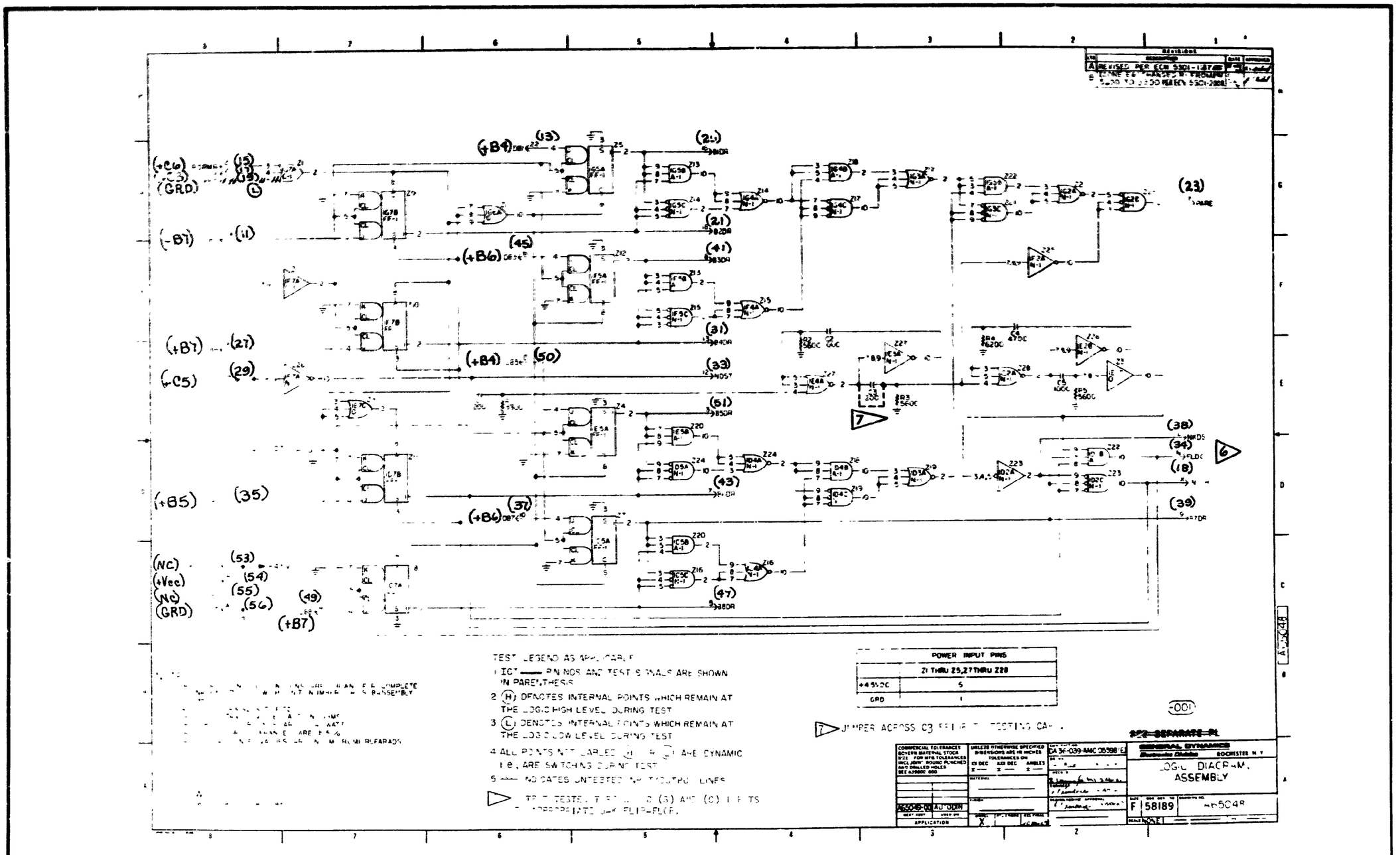


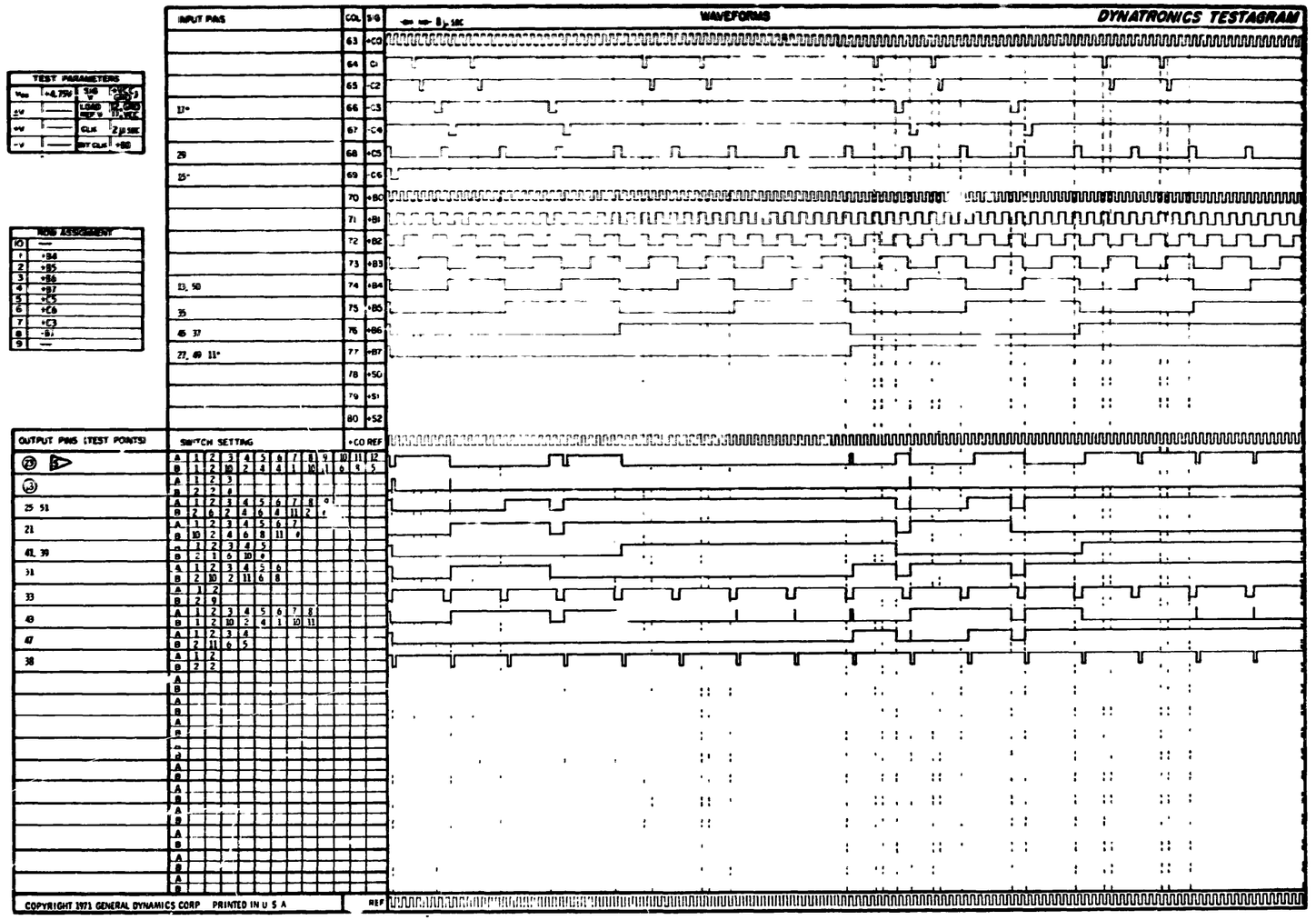
A65045-001 DOC. NO. 23-2113-22

GOVT APPD. JN DATE 7-6-71

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. JUMPER ACROSS C1 AND C3 PRIOR TO TEST.


(+C6)
(GRD)
(-B7)
(+B7)
(+C5)
(+B5)
(NC)
(+Vcc)
(NC)
(GRD)
(+B4)
(+B6)
(+B4)
(+B6)
(+B7)
(13)
(45)
(50)
(35)
(53)
(54)
(55)
(56)
(49)
(21)
(41)
(31)
(33)
(51)
(43)
(37)
(47)
(23)
(38)
(34)
(18)
(39)
TEST LEGEND AS APPLICABLE
1 IC# — PIN NOS. AND TEST SIGNALS ARE SHOWN IN PAREN.THESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) & (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST
5 — NO GATES UNTESTED NO TRI-STATE OUTPUT LINES
TRI-STATE TESTED AT (H) AND (L) INPUTS AS APPROPRIATE FOR FLIP-FLOP.
POWER INPUT PINS
Z1 THRU Z5,Z7 THRU Z28
+4.5VDC 5
GRD 1
JUMPER ACROSS C3 FOR IC TESTING ONLY
-001
SEE SEPARATE PL
GENERAL DYNAMICS
Electronics Division ROCHESTER, N.Y.
LOGIC DIAGRAM, ASSEMBLY
DA 34-039-AMC 06598(E)
F 58189
A5048-001 AUDIN
APPLICATION
A5048



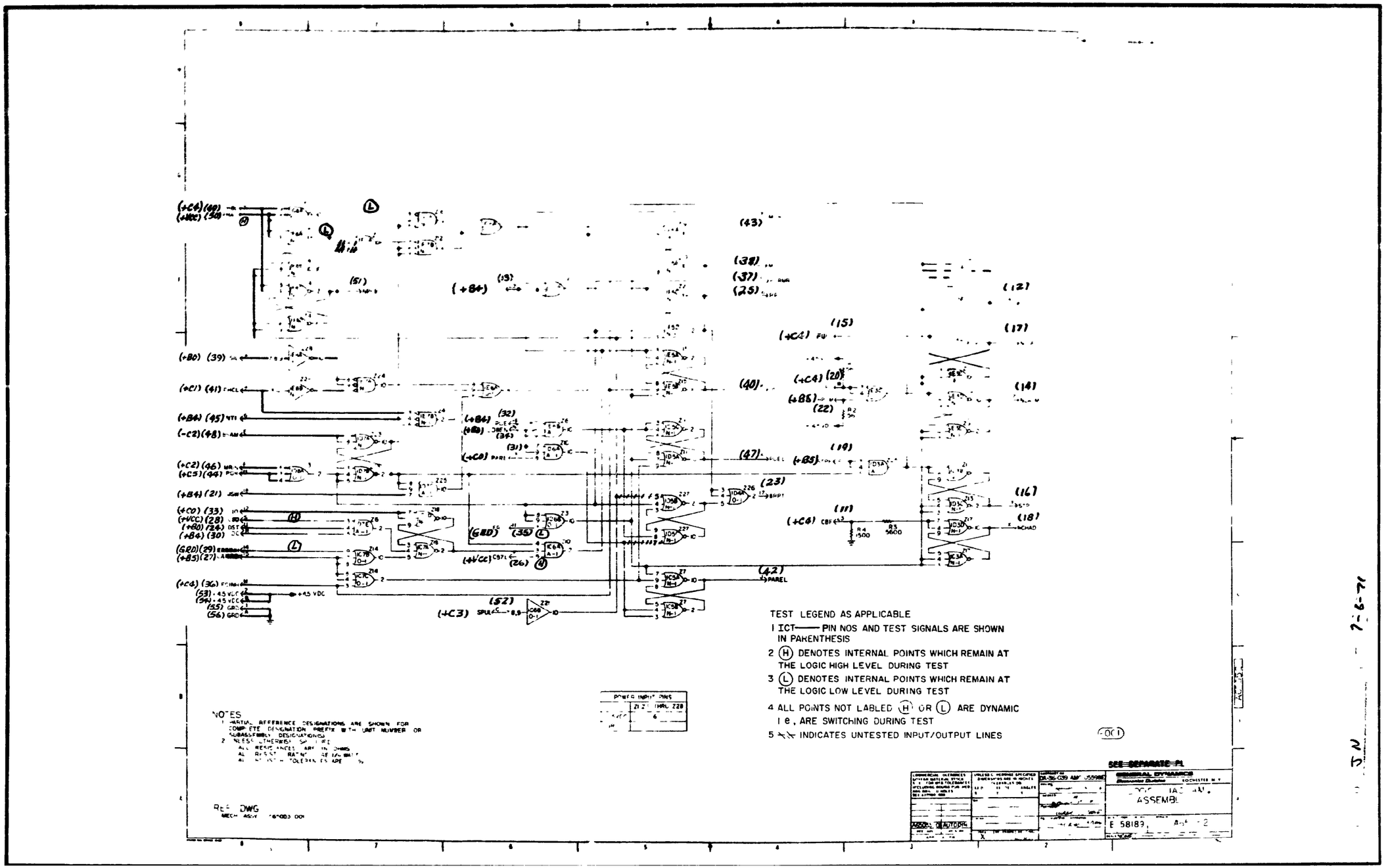
A65049-001 DOC. NO. 23-2114-11

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO 4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

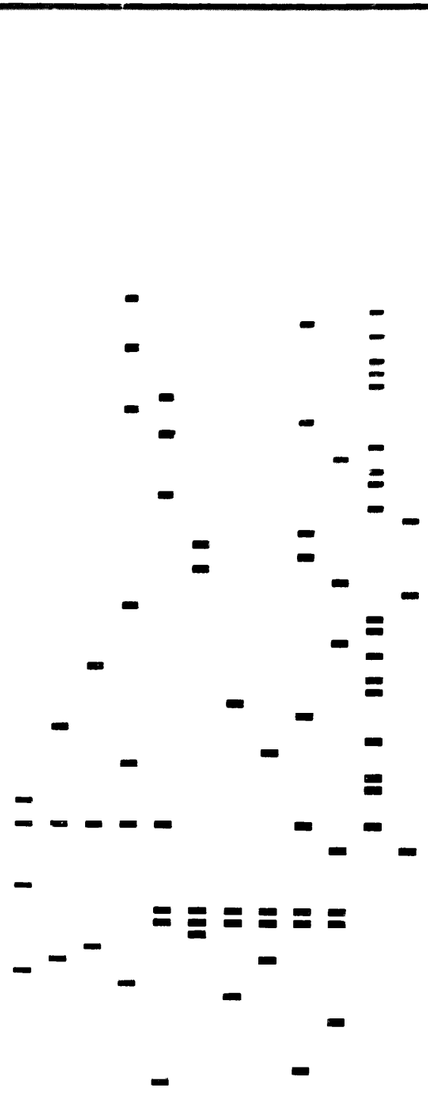
5> JUMPER ACROSS C3 PRIOR TO TEST.



P. C. Assembly A65053

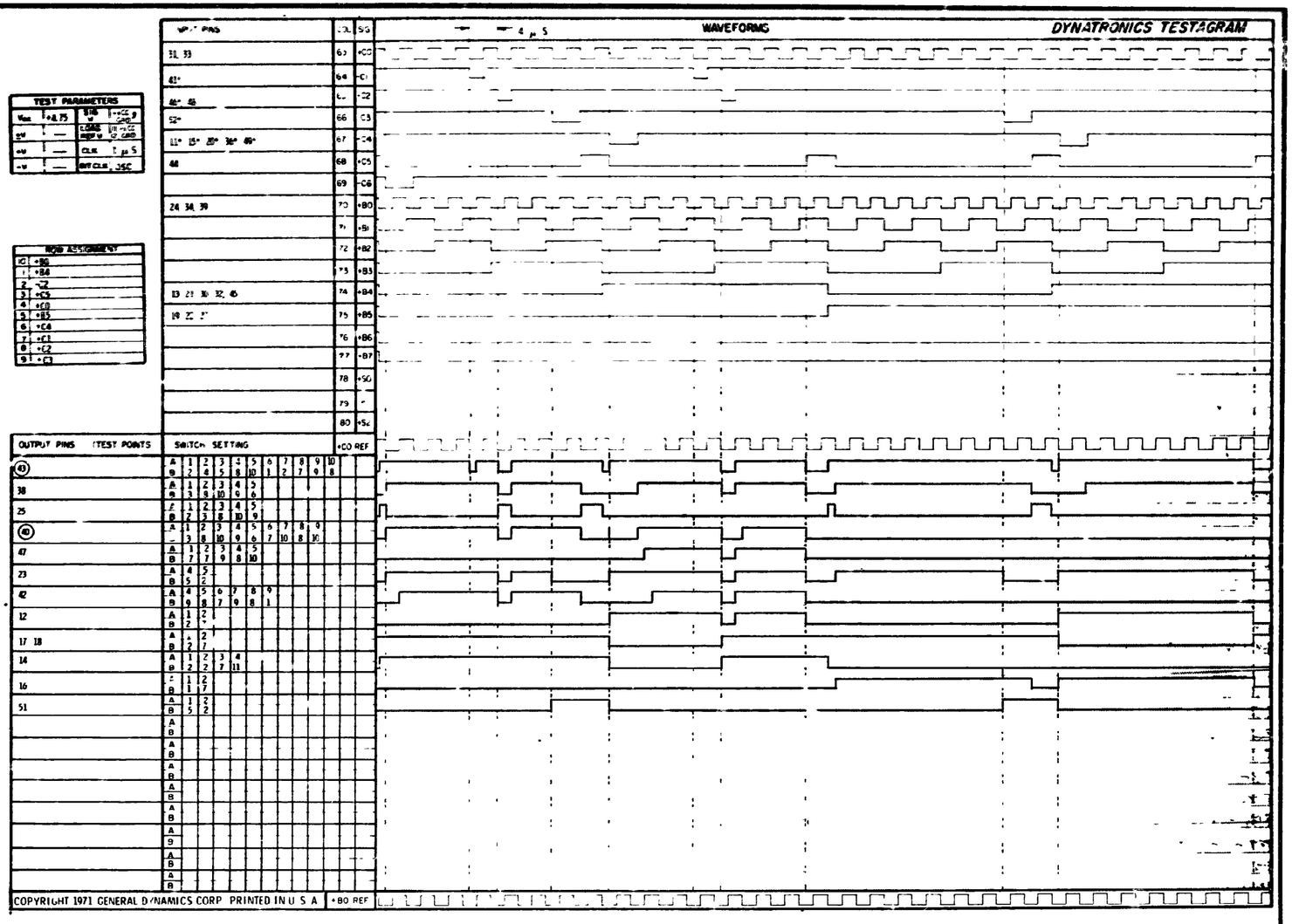
F. C. Logic A65152

Doc. No. 23-2115-12



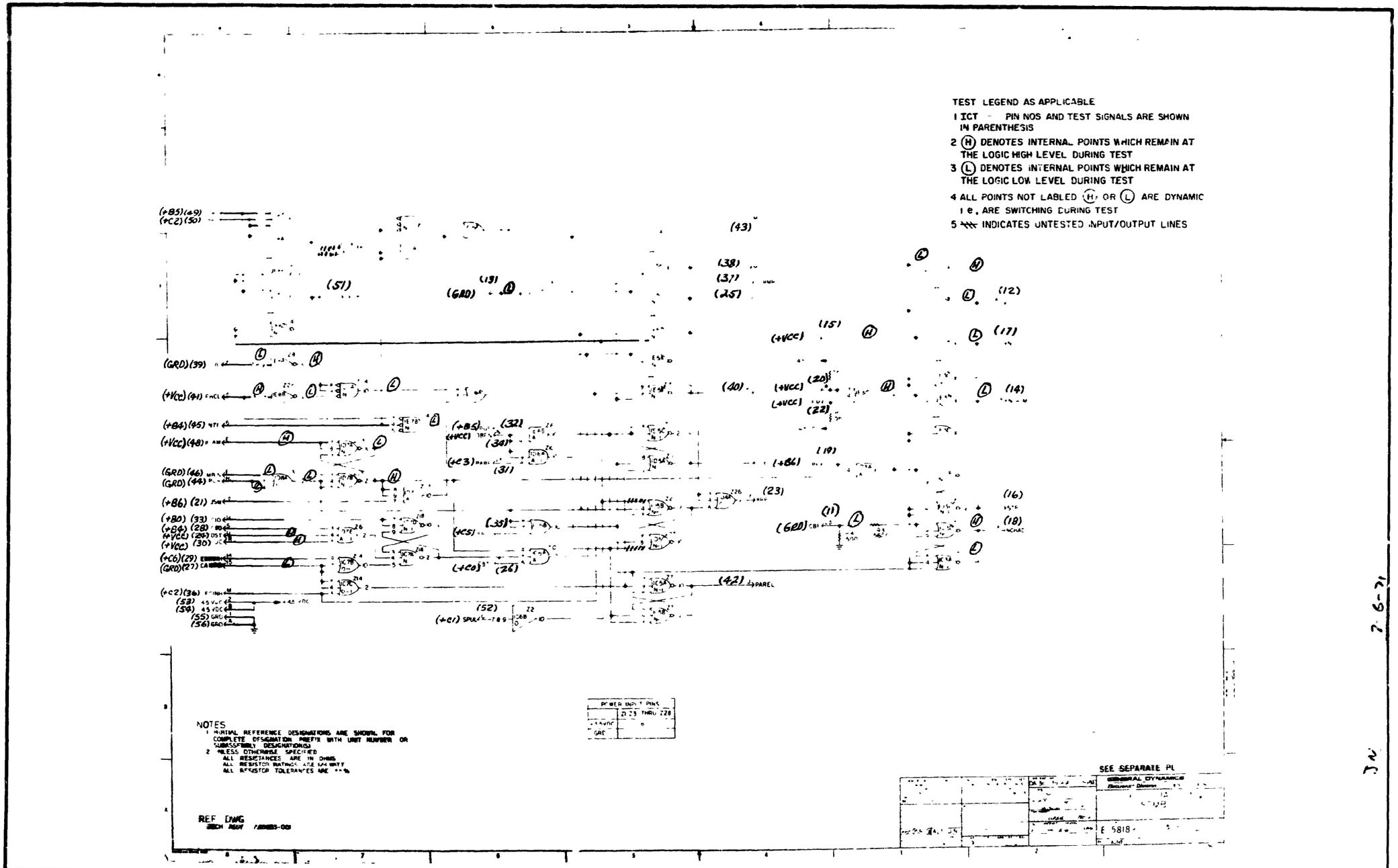
A65053-001 DOC. NO. 23-2115-12

GOVT APPD. JN DATE 7-6-71

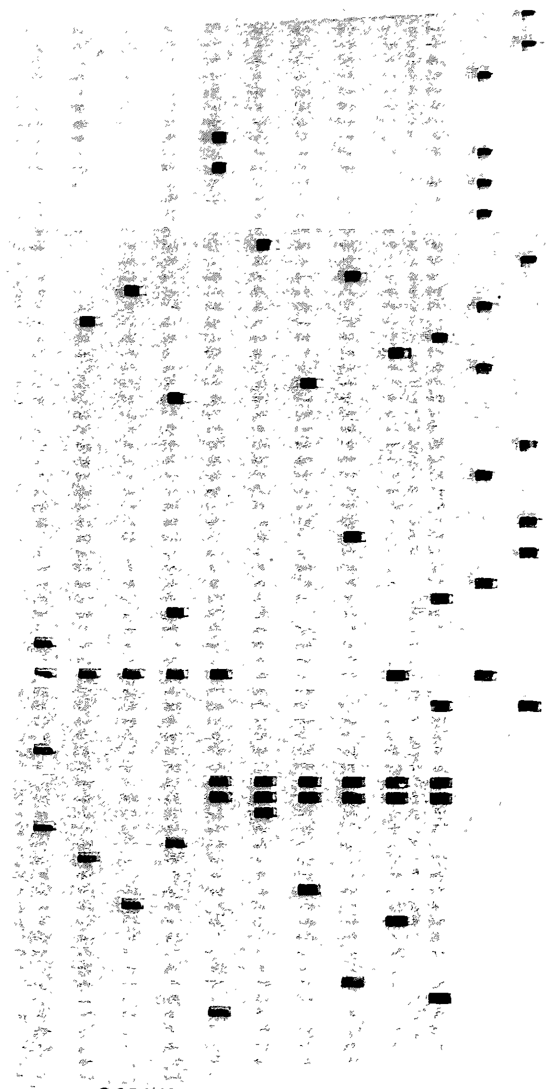


NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO FIRST.



P.C. Assembly A65053
P.C. Logic A65052

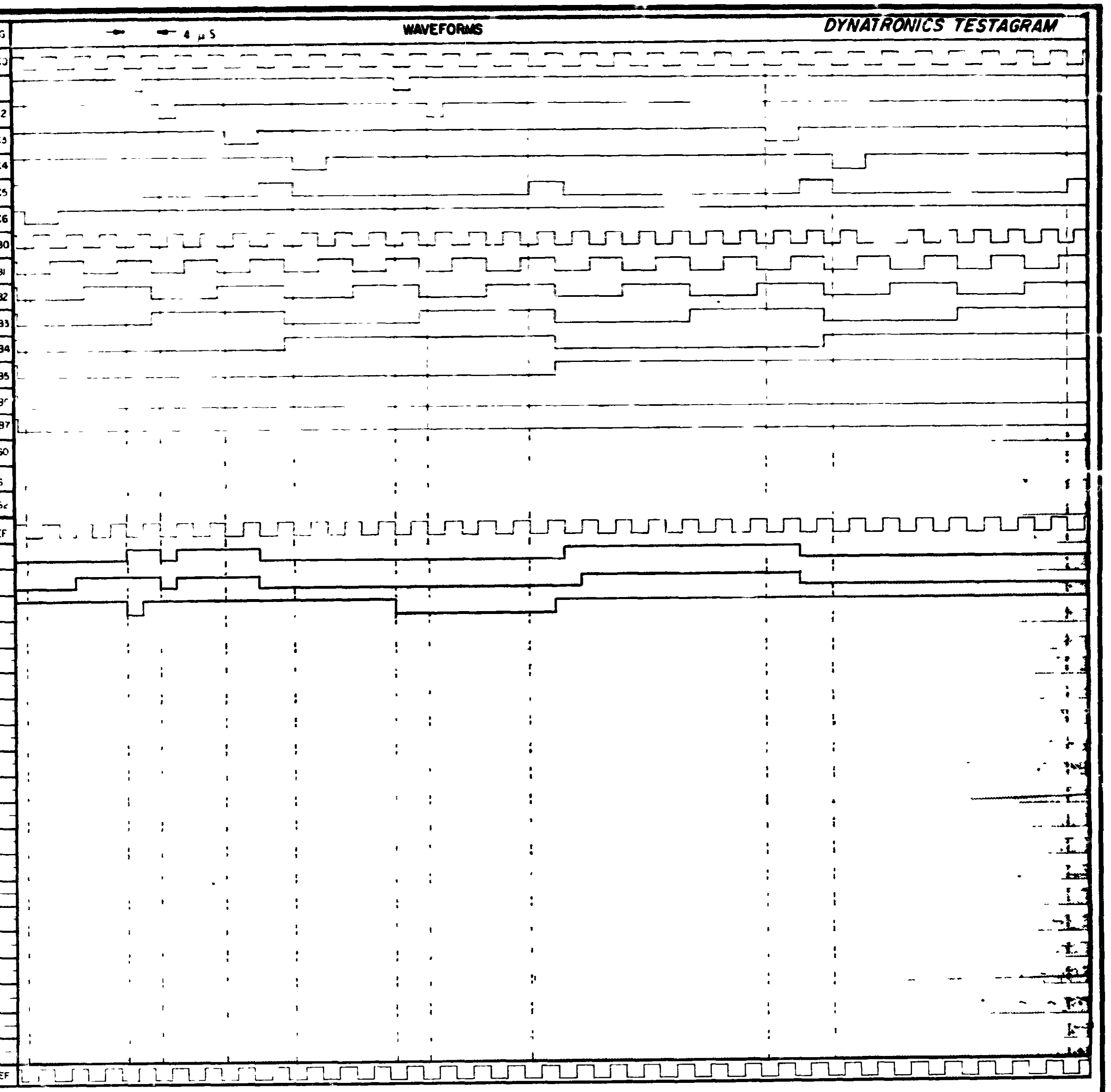


TEST PARAMETERS			
V_{cc}	+4.75	SIG V	+VCC, GND
±V	—	LOAD REF V	+VCC, ±GND
+V	—	CLK	1 µS
-V	—	BIT CLK	OSC

ROW ASSIGNMENT	
0	+B5
1	+B0
2	+B4
3	+C5
4	+C0
5	+B6
6	+C2
7	+C6
8	+C3
9	+C1

INPUT PINS	COL	SIG
2*	63	+C0
52*	64	-C
3c* 50*	65	C2
31*	66	C3
	67	-C4
35	68	+C5
29*	69	-C6
33	70	+B0
	71	+B1
	72	+B2
	73	+B3
28, 45	74	+B4
32, 49	75	+B5
18, 21	76	+B6
	77	+B7
	78	+S0
	79	+S
	80	+S2

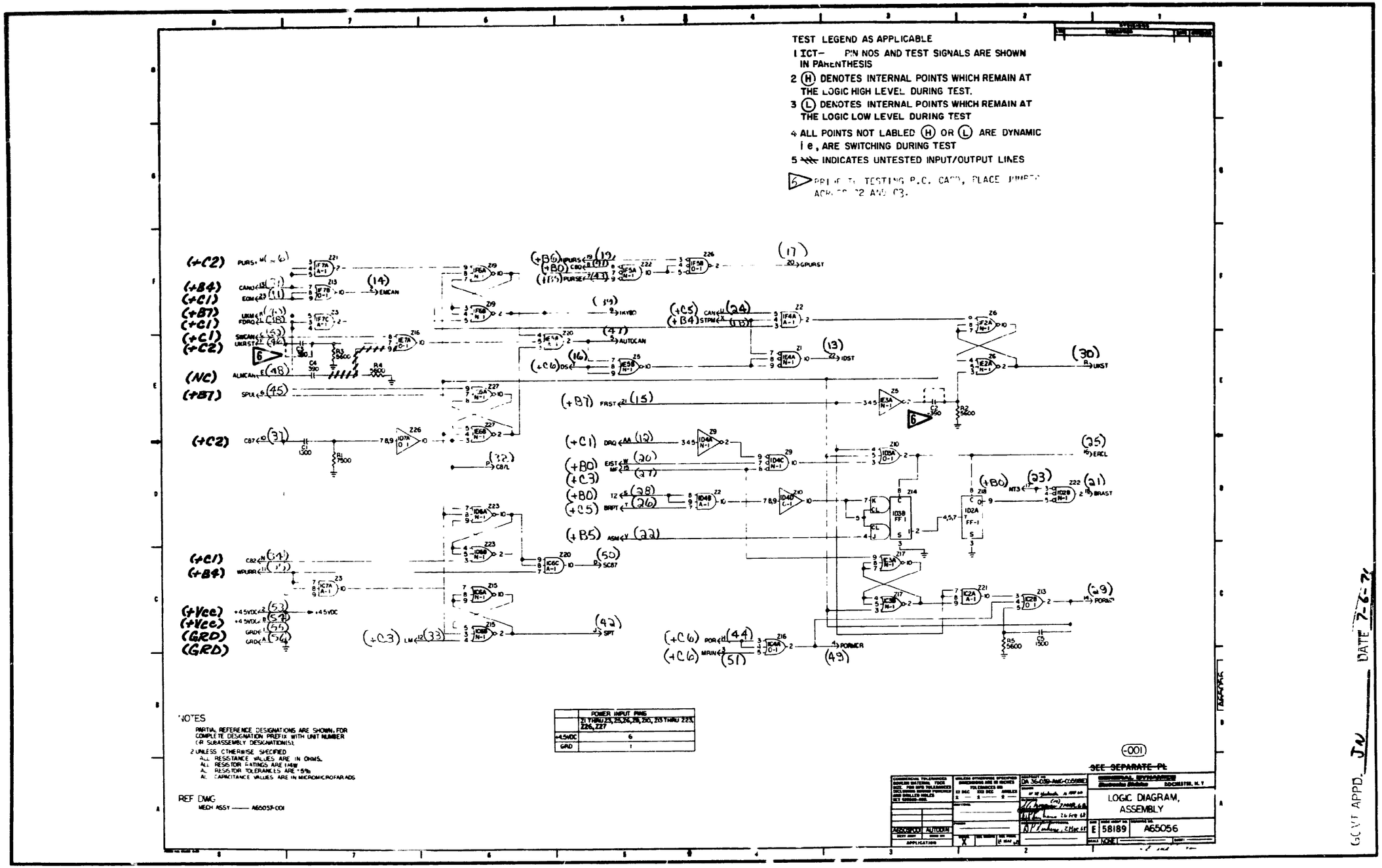
OUTPUT PINS (TEST POINTS)	SWITCH SETTING						
38	A	1	2	3	4	5	6
	B	4	8	10	9	1	7
40	A	1	2	3	4	5	
	B	9	8	10	9	3	
23	A	1	2	3	4		
	B	4	6	3	11		



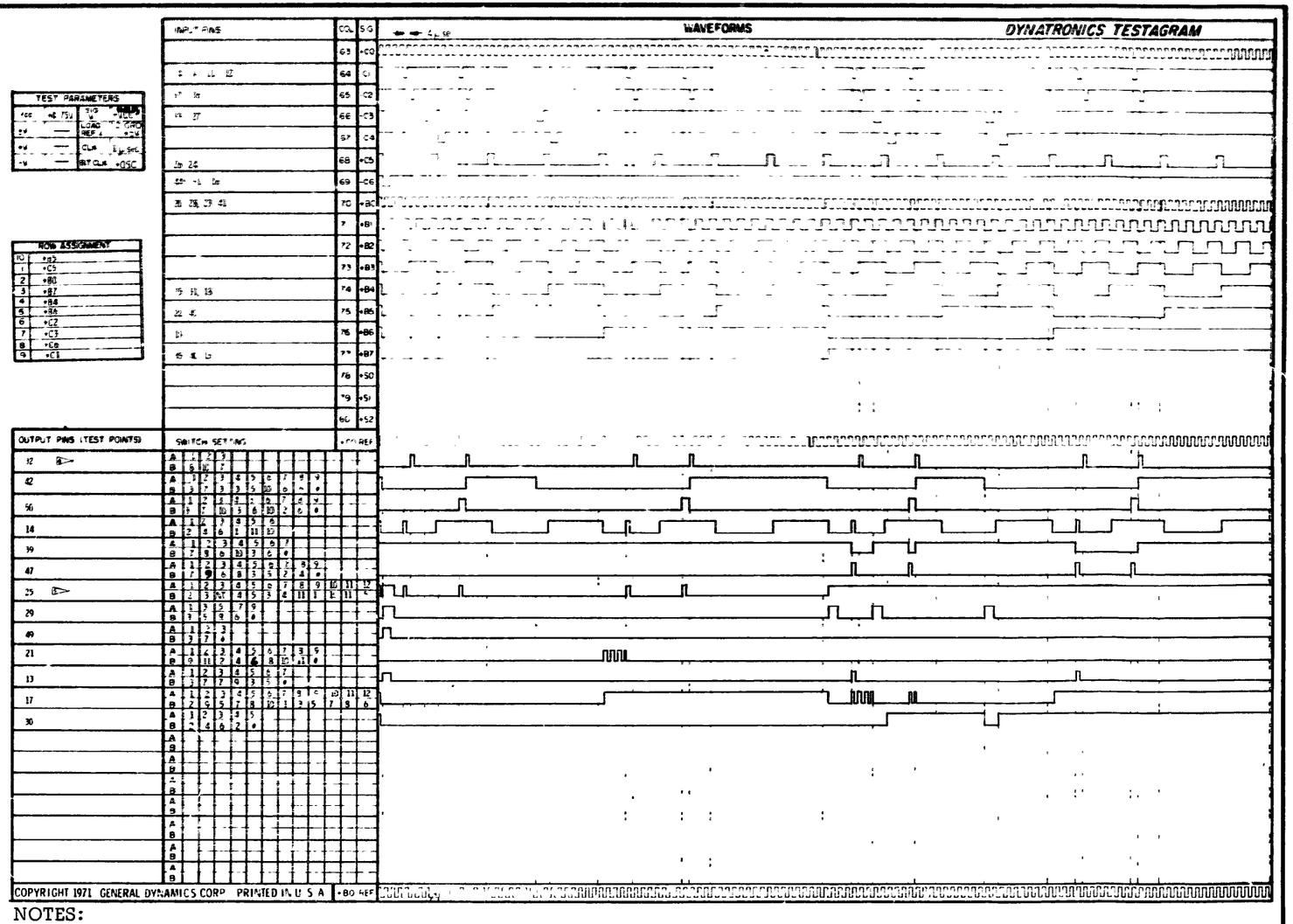
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

GOVT APPD. JN DATE 7-6-71



P.C. Assembly A65057-001



NOTES:

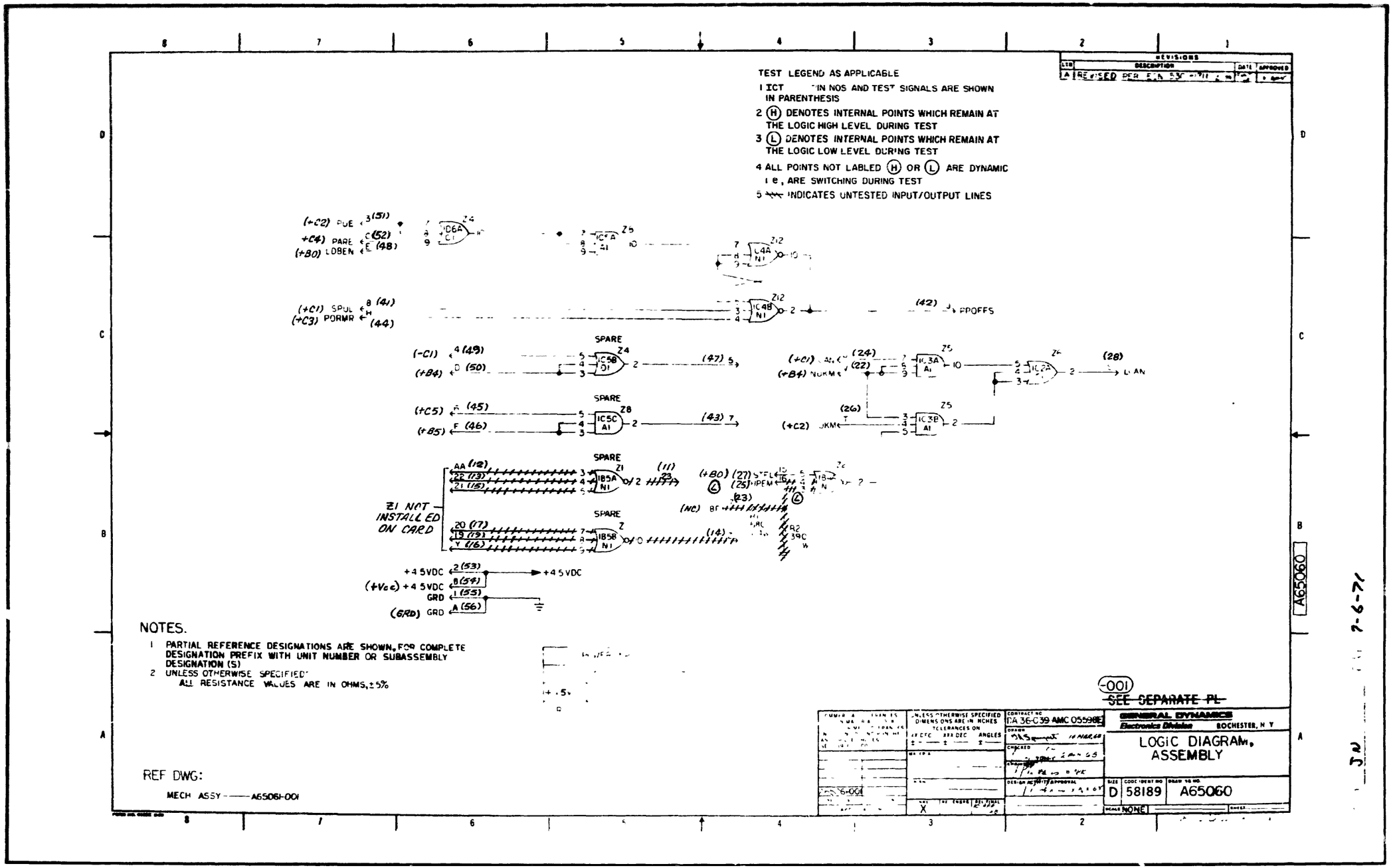
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.

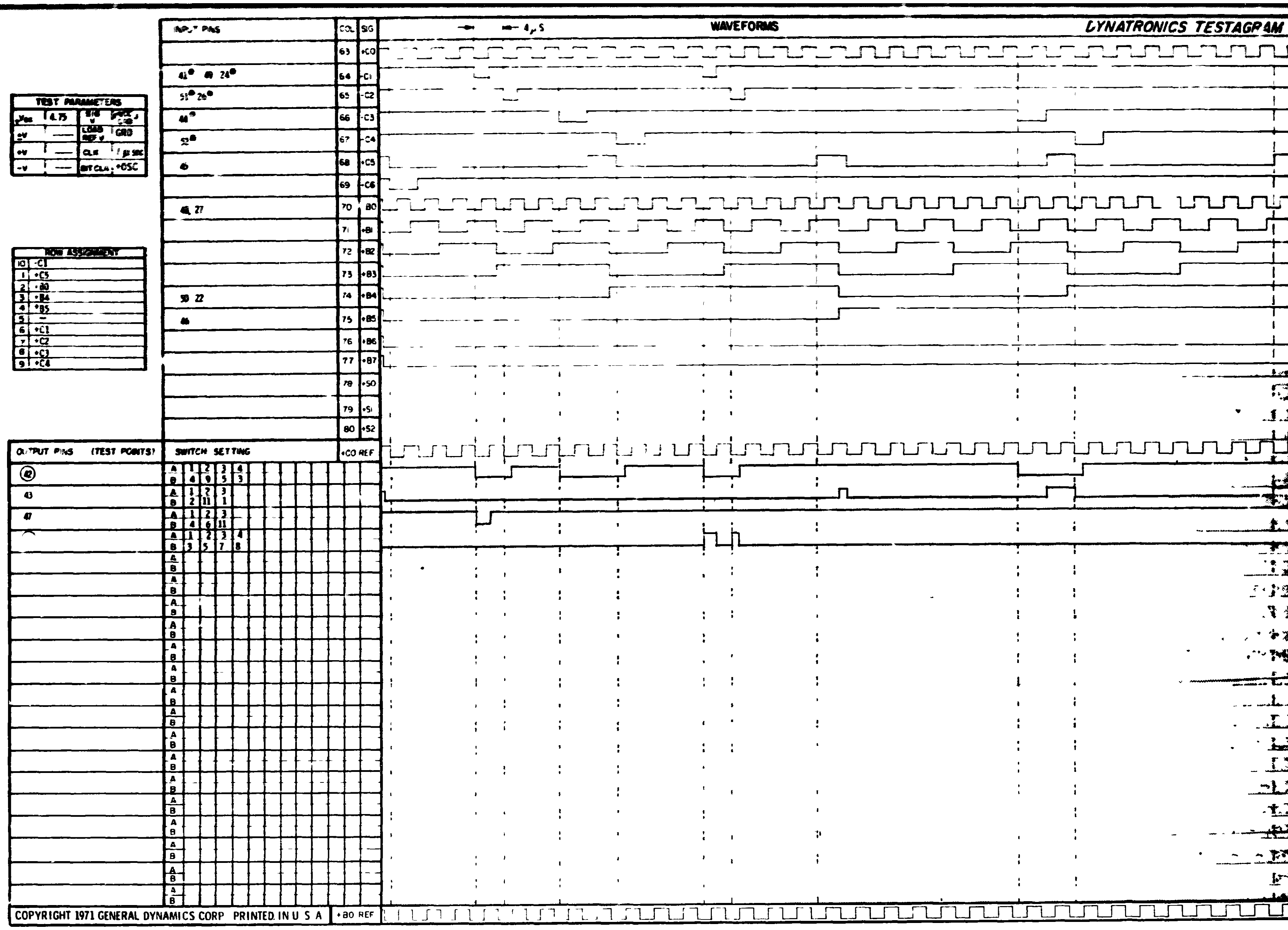
4. PRIOR TO TESTING PC CARD PLACE A JUMPER ACROSS CAPACITORS C2 & C3.
5. NT MEANS NO TEST FOR "A" SWITCH POSITION 3.

A65057-001 DOC. NO. 23-2116-11

T APPD. JW DATE 7-6-71



P.C. Assembly A65061-001

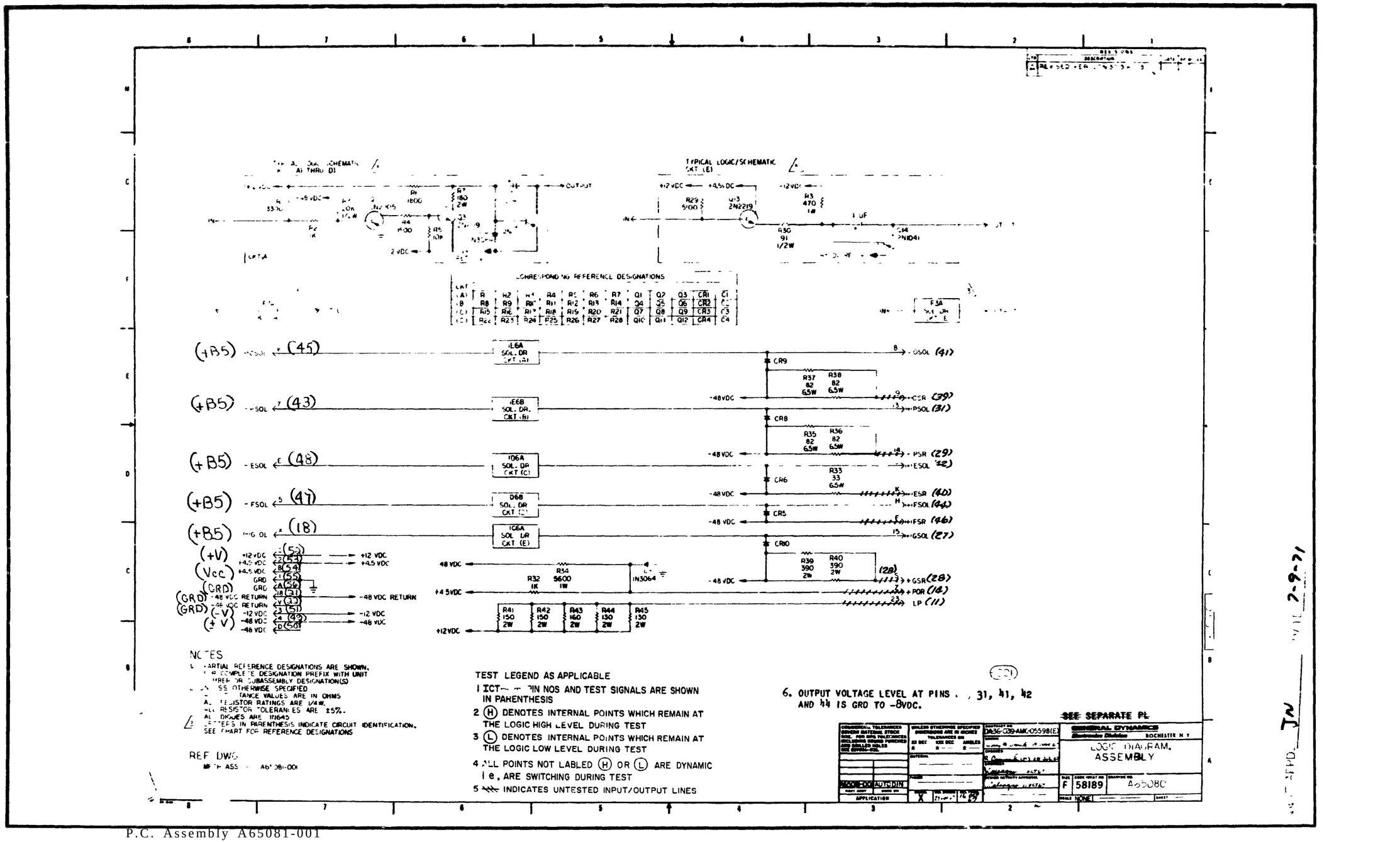


A65061-001 DOC. NO. 23-2117-11

GOVT APPD. JN DATE 7-6-71

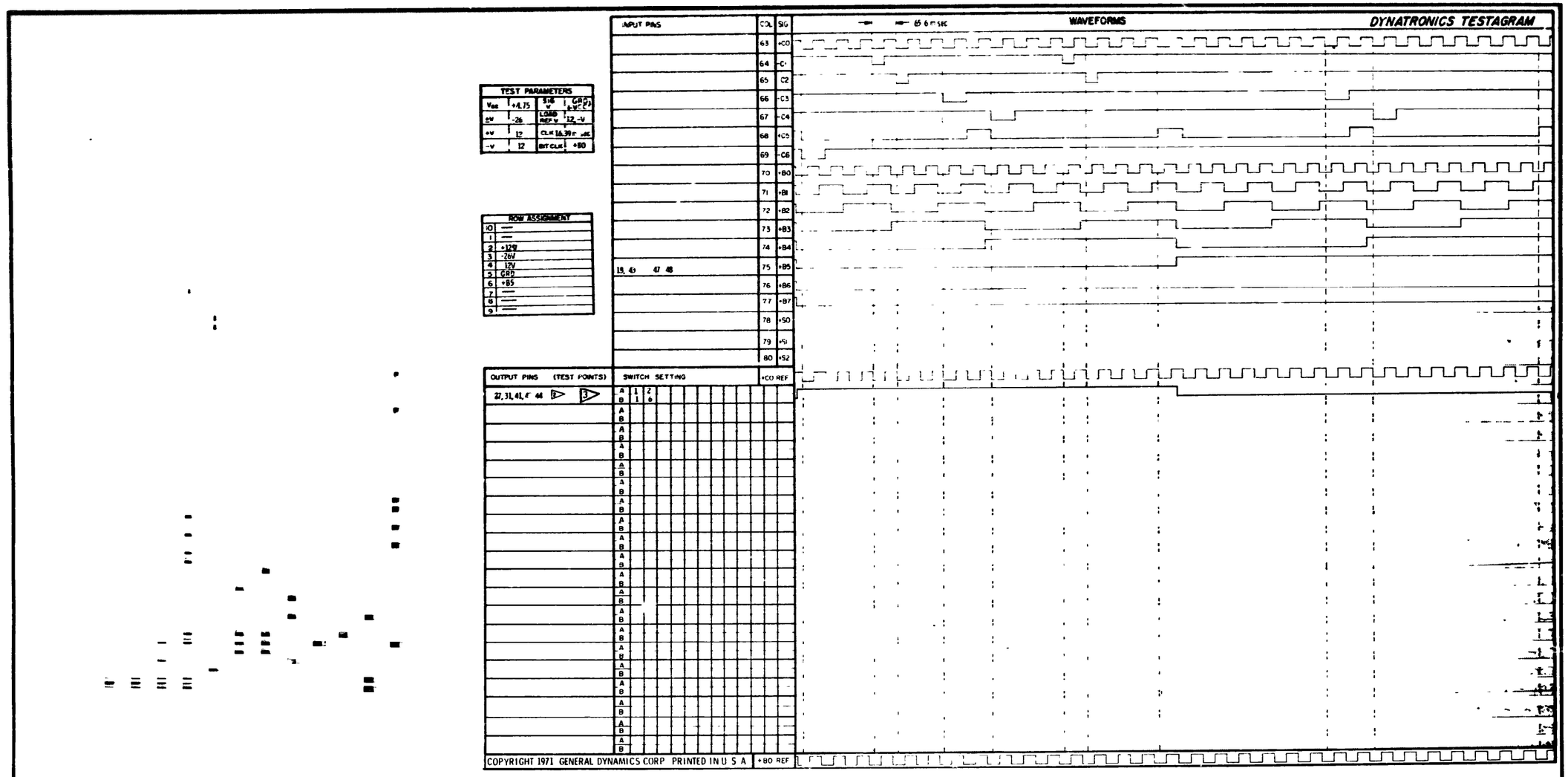
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. SPARE GATES ON SCHEMATIC WHICH ARE NOT INSTALLED ON BOARD ARE NOT PROGRAMED.



P.C. Assembly A65081-001

P.C. Logic A65080 Doc. No. 23-2118-11



NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. OUTPUT VOLTAGE LEVELS AT PINS 27, 31, 41, 42, 44 ARE GRD TO -8 VDC.
3. GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.

A65081-001 DOC. NO. 23-2118-11

GOVT APPD. JN DATE 7-9-71

TEST LEGEND AS APPLICABLE

1 ICT- PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

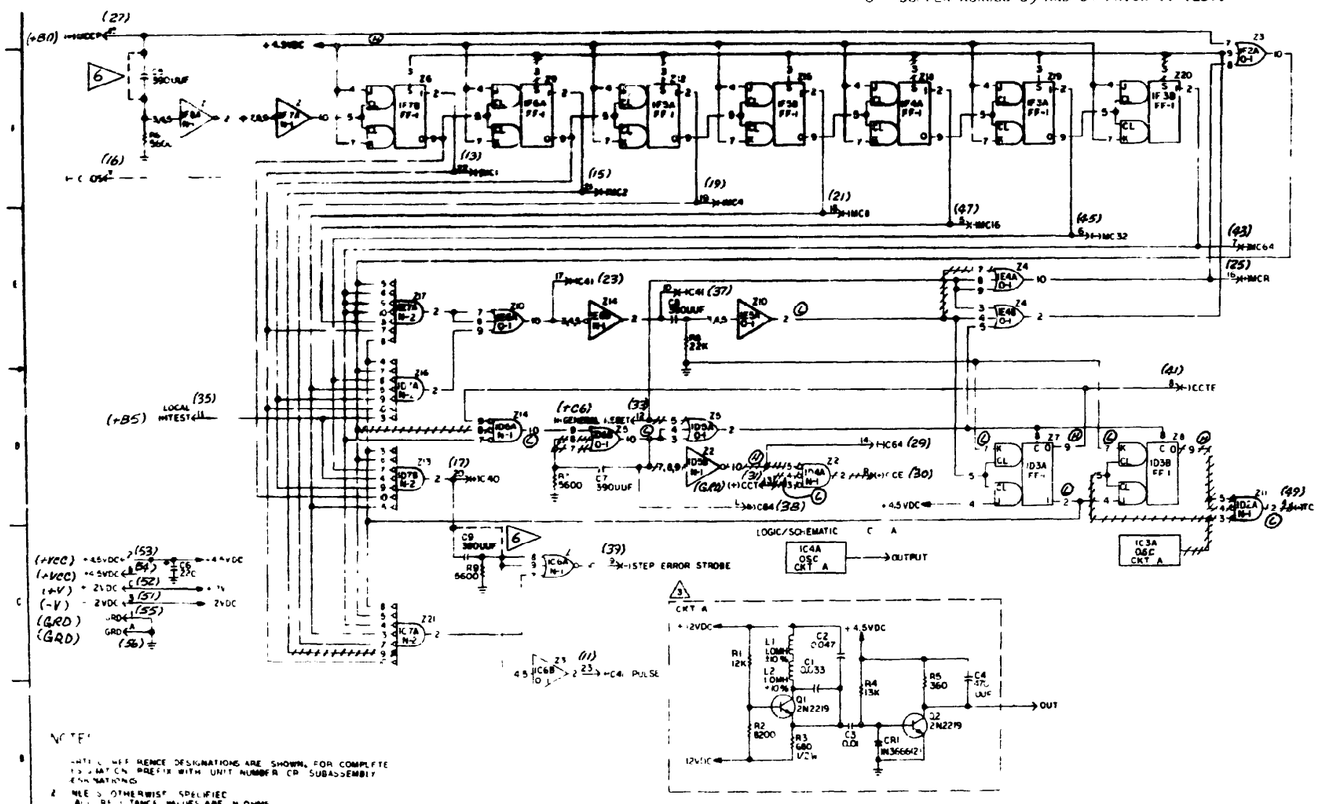
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i e , ARE SWITCHING DURING TEST

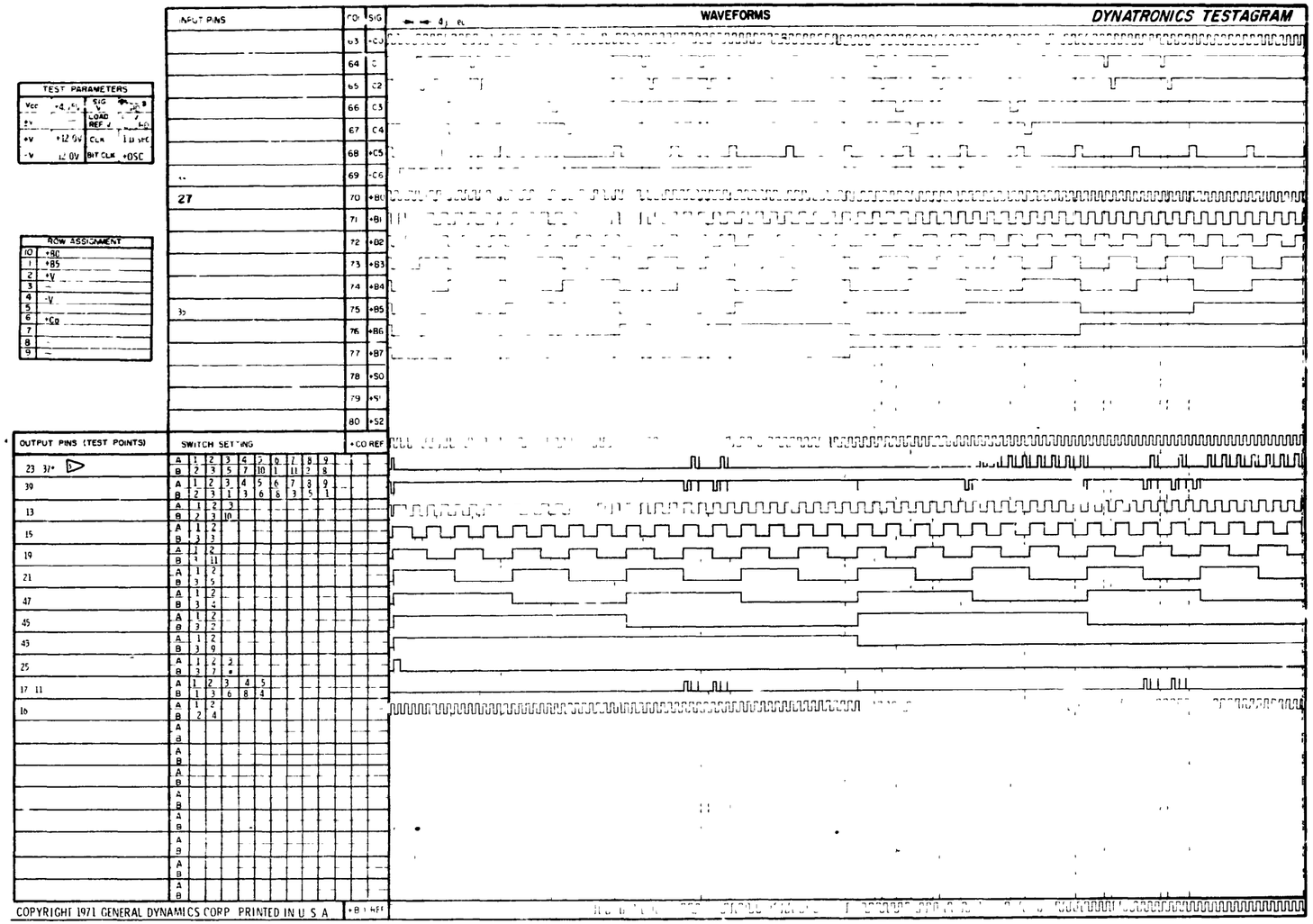
5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES

6 JUMPER ACROSS C5 AND C9 PRIOR TO TEST.



NOTE:

REF DWG



A65085-001 DOC. NO. 23-2119-12

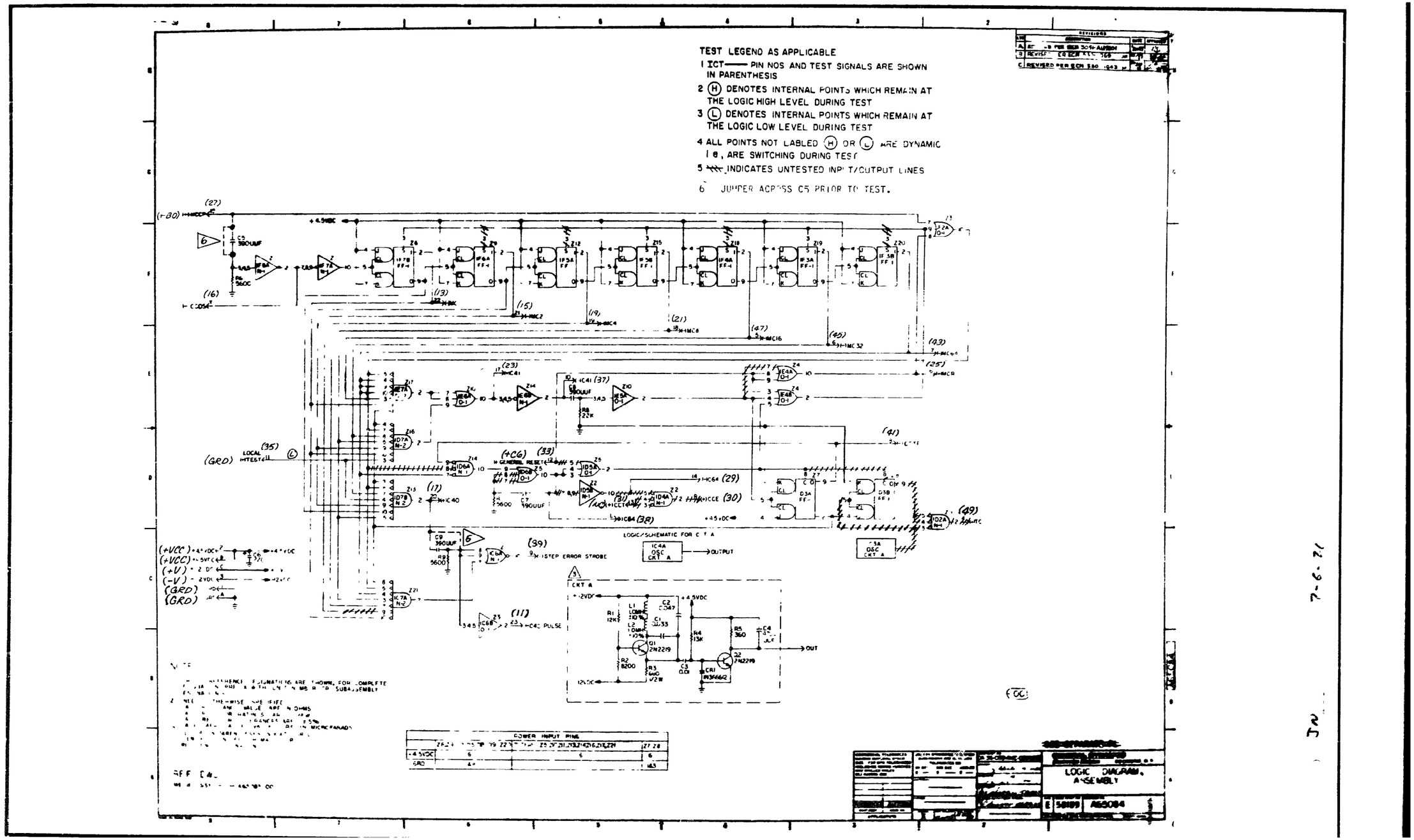
GOVT APPD. JN DATE 2-6-71

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

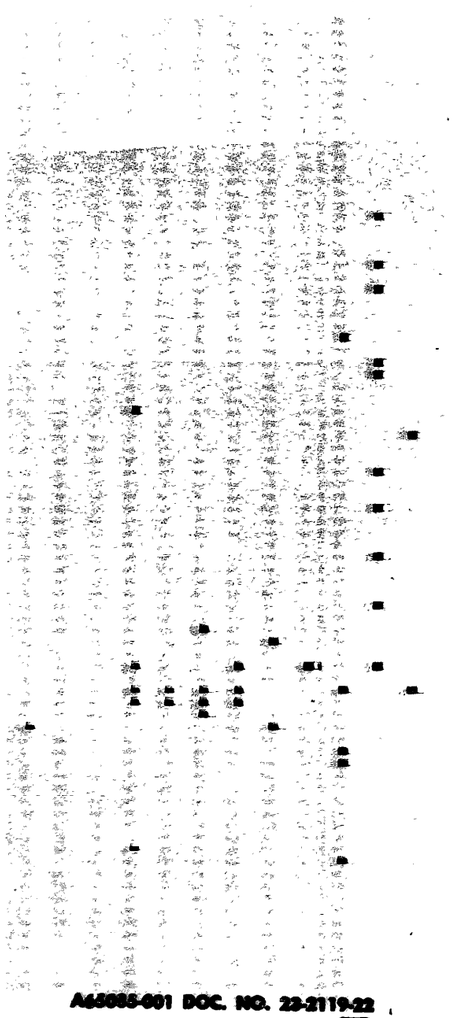
5 JUMPER ACROSS C5 AND C9 PRIOR TO TEST.



P.C. Assembly A65085

134 P.C. Logic A65084

Doc. No. 22-2119-22



A65085-001 DOC. NO. 23-2119-22

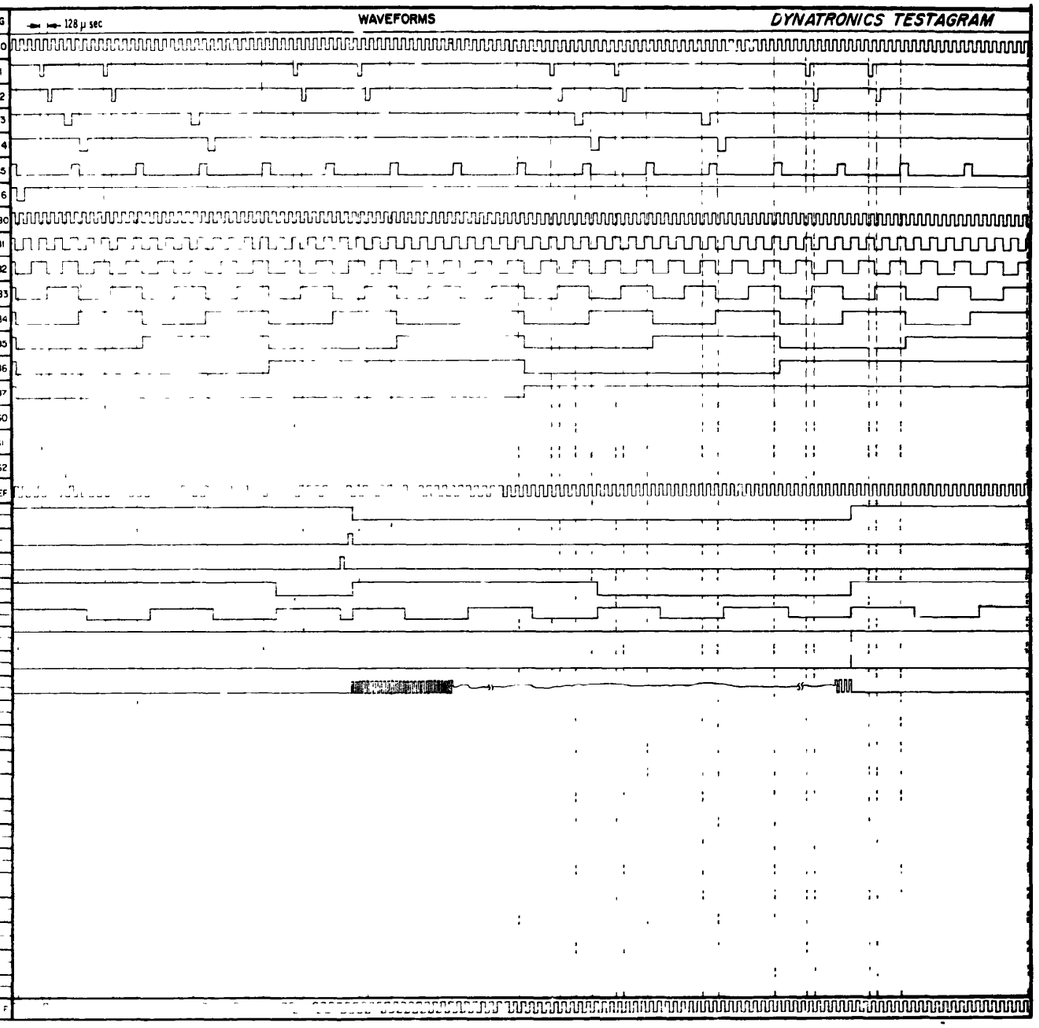
IT APPD. JN DATE 7-6-71

TEST PARAMETERS			
V_{CC}	+4.75V	SIG V	VOLT. GRD
±V	—	LOAD REF V	11, VCC 12, C0
+V	+12.0V	CLK	32 µsec
-V	12.0V	BIT CLK	+OSC

ROW ASSIGNMENT	
10	+60
1	—
2	+V
3	—
4	V
5	—
6	+C0
7	—
8	—
9	—

INPUT PINS	COL	SIG
	63	+C0
	64	C1
	65	-C2
	66	-C3
	67	C4
	68	+C5
33*	69	-C6
27	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING	+C0 REF
(41) ▷		
23		
1*		
45		
21		
29 (REF ONLY)		
38 30 (REF ONLY)		
49 (REF ONLY)		



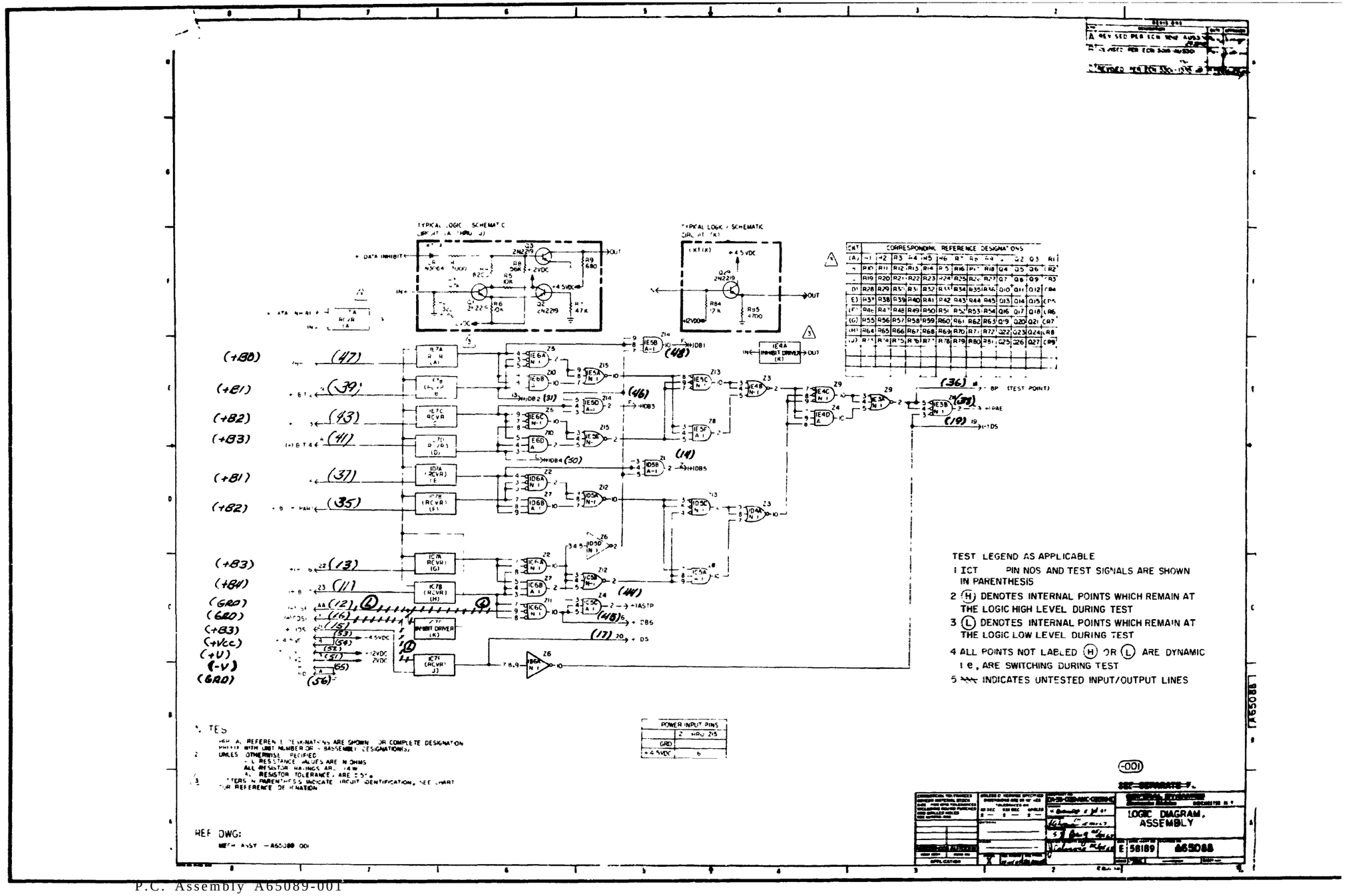
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

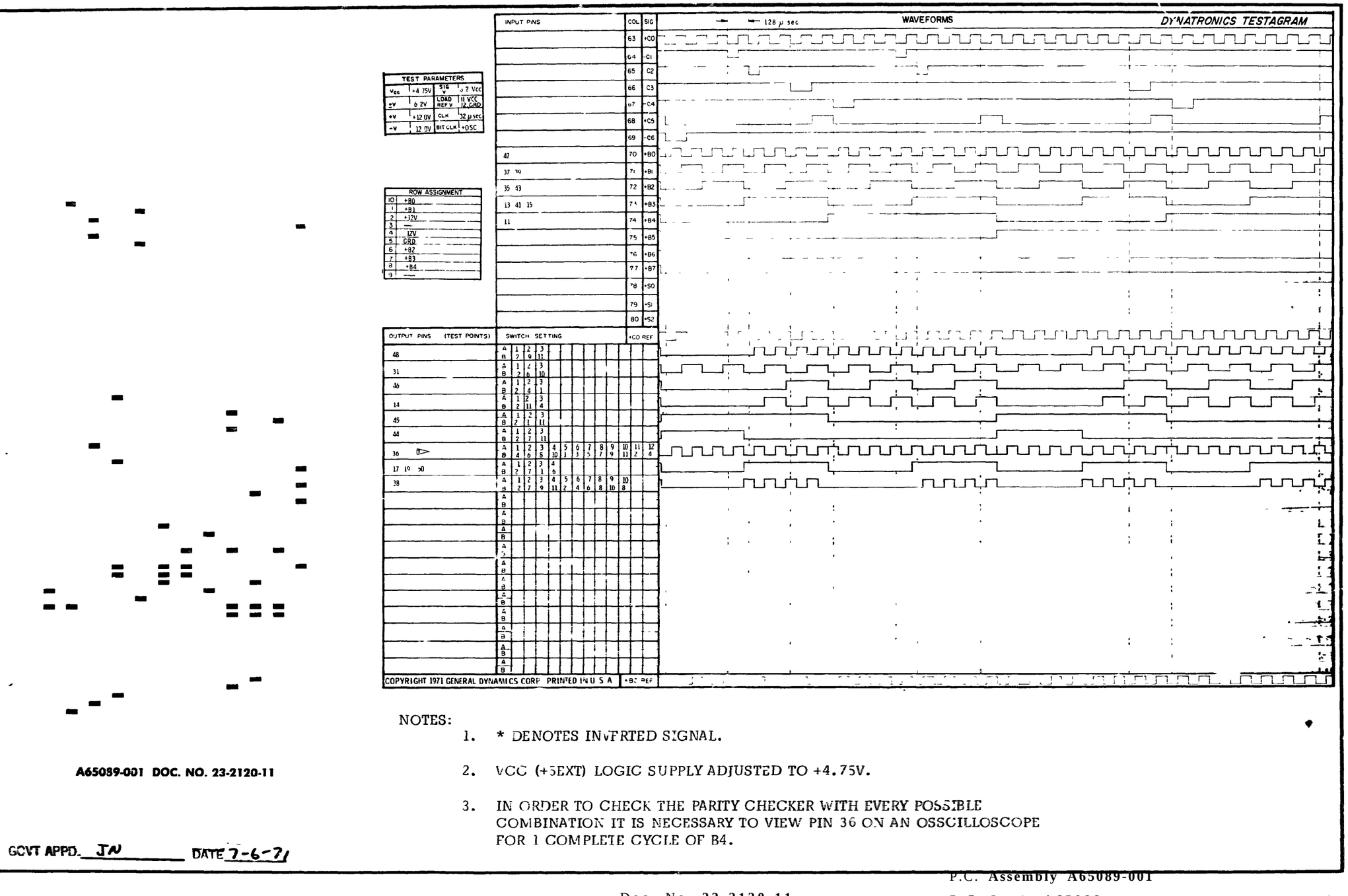
5 ▷ JUMPER ACROSS C5 PRIOR TO TEST.

6. WAVEFORMS FOR OUTPUT PINS 22, 30, 38, 49 ARE FOR REFERENCE.



P.C. Assembly A65089-001

136 P.C. Logic A65088 **Doc. No. 23-2120-11**



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ORDER TO CHECK THE PARITY CHECKER WITH EVERY POSSIBLE COMBINATION IT IS NECESSARY TO VIEW PIN 36 ON AN OSSCILLOSCOPE FOR 1 COMPLETE CYCLE OF B4.

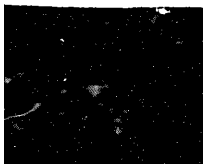
A65089-001 DOC. NO. 23-2120-11

GOVT APPD. JW DATE 7-6-71

END

02-05-83

DATE



DEPARTMENT OF THE ARMY

MICROFORM
TEST TARGET